SPI Nand Datasheet

3.3V 1Gbit (128MByte)

Revision History

RevisionNo.	History	Date
1.0	First Release	Sep 2021

1 Overview

1.1 Feature

1G-bit SPI NAND FLASH

Page size : (2K+64spare) bytes

Block size : (128K+4K) bytes

Device size: 1024 blocks

Advanced Security Features

8K-Byte OTP region

Support Standard, Dual, and Quad SPI

Standard SPI: SCLK, CS#, SI, SO, WP#, HOLD#

Dual SPI: SCLK, CS#, SIO0, SIO1, WP#, HOLD#

Quad SPI: SCLK, CS#, SIO0, SIO1, SIO2, SIO3

High Clock Frequency

Quad I/O data transfer up to 320Mbits/s

2048/64/16 wrap read option

Program/Erase/Read Cycle Time

Page read time: 250us Maximum(w/I ECC)

Page program time: 400us typical

Block erase time: 3ms typical

Software/Hardware Write Protection

Software protection of the entire device or ranges of blocks

Hardware protection through WP#

High Access Performance with Cache

Cache size: 1024 bytes

ECC Protection

8 bits ECC for each 512 bytes

Enhanced Functions

Synchronous output of internal reset signals (custom-made)

Data in Block 0/Page 0 automatically loads to the cache after power up

Excellent Electrical Performance

Single supply voltage: 2.7~3.6V

Operating current < 20mA

Standby current < 100uA

Commercial Standard

Operating temp: -20℃ to 85℃

Storage temp: -65℃ to +150℃

2 General Description

The MKSV1GCL-AC is 1G-bit with spare 64Mbit capacity. The device is offered in 3.3V power supply. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. The memory is divided into blocks that can be erased independently so it possible to preserve valid data while old data is erased. The device contains 1024 blocks, composed by 64 pages consisting in two NAND structures of 32series connected Flash Cells. A program operation can be performed in typical 400us on the 2048-bytes and an erase operation can be performed in typical 3ms on a 128K-bytes block. The on- chip write control automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. Even the write-intensive systems can take advantage of the MKSV1GCL-AC's extended reliability of 100K program/erase cycles by providing ECC (Error Correction Code) with real time mapping-out algorithm.

MKSV1GCL-AC features a serial peripheral interface and software protocol allowing operation on a simple 3- wire bus while it is in single I/O mode. The three signals are a clock input (SCLK), a serial data input(SI), and a serial data output (SO). Serial access to the device is enabled by CS# input. When it is in four I/O read mode, the SI pin, SO pin, WP# pin and HOLD# pin become SIO0 pin, SIO1 pin, SIO2 pin SIO3 pin for address/dummy bits input and data output.

The copy back function allows the optimization of defective blocks management : when a page program operation fails the data can be directly programmed in another page inside the same array section without the time consuming serial data insertion phase. The MKSV1GCL-AC is an optimum solution for large nonvolatile storage applications such as solid state file storage and other portable applications requiring non-volatility.

After program/erase command is issued, auto program/erase algorithms which program/erase and verify the specified page or sector/block locations will be executed. Up to 2Kbytes can be programmed at a time. Pages can be erased in groups of 128KB erase. To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via OIP bit. Advanced security features enhance the protection and security functions, please see security features section for more details.

The MKSV1GCL-AC supports JEDEC standard manufacturer and device identification with a 8K bytes (4 pages) Secured OTP.

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0).

2.1 Block Diagram

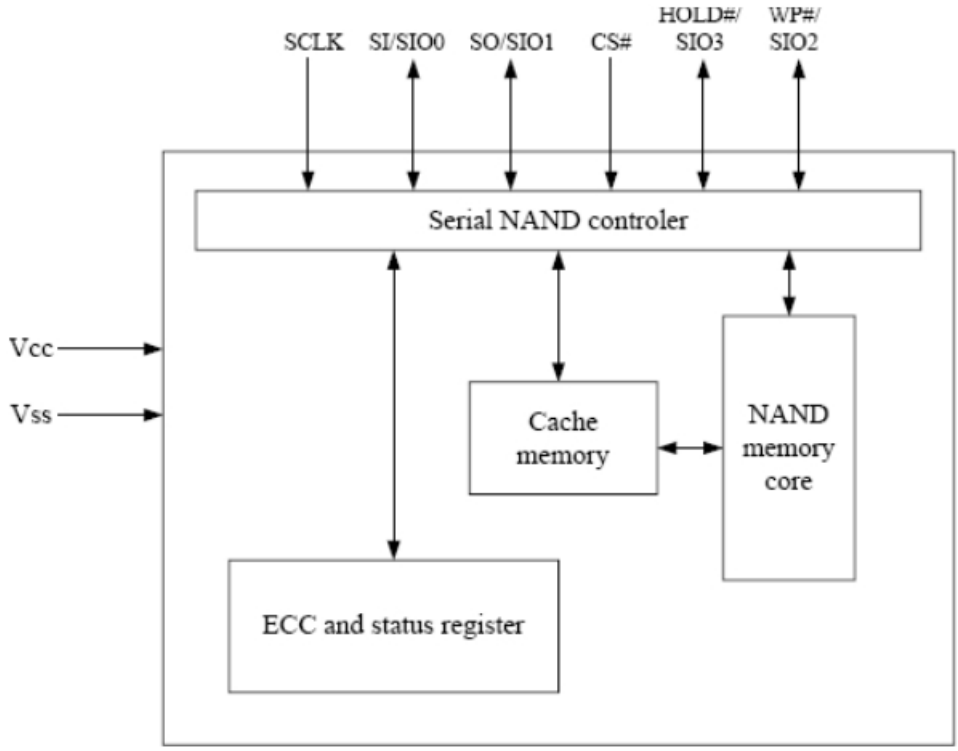


Figure 2-1 Block Diagram of SPI NAND Flash Memory

2.2 Array Organization

Table 2-1 Array Organization of 1G SPI NAND FLASH

Capacity	Page Organization	Block Organization	Block Organization
1Gbits	(2K+64) Bytes	64pages	1024 Blocks

2.3 Memory Address Mapping

Figure 2-2 show the memory address mapping of the 64-page-per-block

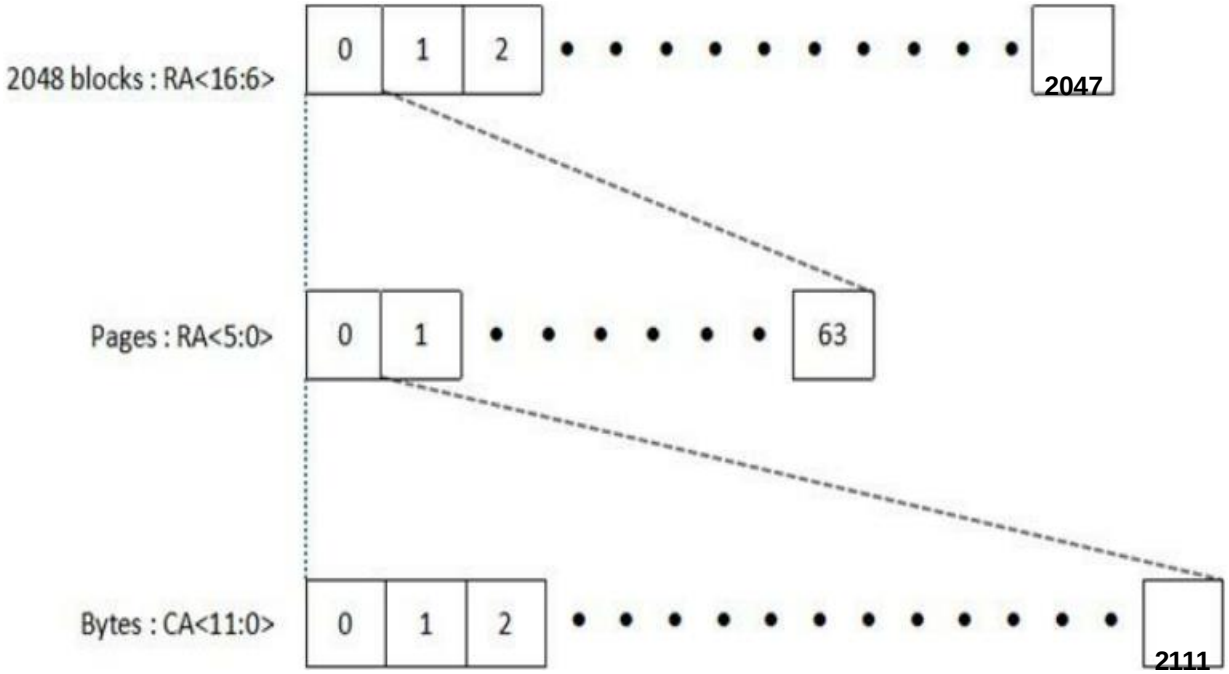


Figure 2-2: Memory Map

Notes:

1. CA: Column Address. The 12-bit address is capable of addressing from 0 to 4095 bytes; however, only bytes 0 through 2111 are valid. Bytes 2112 through 4095 of each page are “out of bounds,” do not exist in the device, and cannot be addressed.

2. RA: Row Address. RA<5:0> selects a page inside a block, and RA<16:6> selects a block:

2.4 Memory Organization

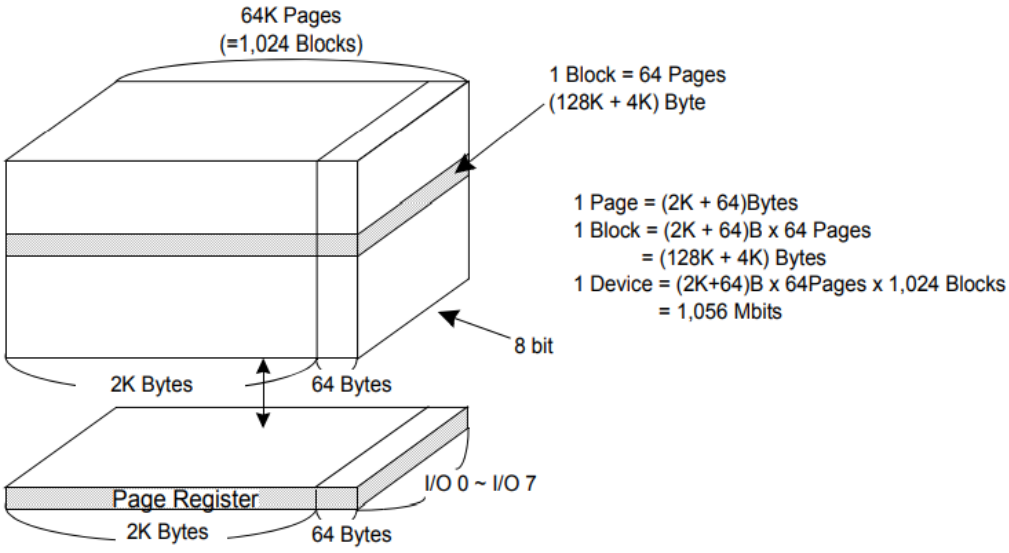


Figure 2-3: Array Organization

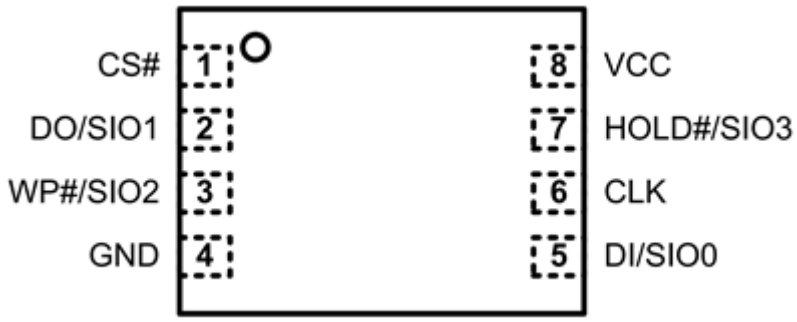
3 Basic Information

3.1 Pin Names

Table 3-1. Pin names

Signal name	Function	Direction
SCLK	Serial Clock	Input
SI(SIO0)	Serial Data Input(for 1 I/O) Serial Data Input& Output(for 4 I/O)	Input / Output
SO(SIO1)	Serial Data Output(for 1 I/O) Serial Data Input& Output(for 4 I/O)	Input / Output
CS#	Chip Select	Input
WP#(SIO2)	Write Protect Serial Data Input& Output(for 4 I/O)	Input / Output
HOLD#(SIO3)	Hold Serial Data Input& Output(for 4 I/O)	Input / Output
VCC	3.3V Supply voltage	
GND	Ground	

3.2 Package



TOP VIEW

Figure 3.1 8 Pad WSON
6X8mm

3.3 Signal Descriptions

Serial Data output (SO) – SIO1

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (SCLK) at all read mode. Also, When the device is Quad mode, this pin(SO) is used for SIO1

Serial Data input (SI) – SIO0

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be programmed. Values are latched on the rising edge of Serial Clock (SCLK). Also, When the device is Quad mode, this pin(SI) is used for SIO0

Serial Clock (SCLK)

This input signal provides the timing of the serial interface. Instructions, addresses, or data present at Serial Data Input (SI) are latched on the rising edge of Serial Clock (SCLK). Data on Serial Data Output (SO) changes after the falling edge of Serial Clock (SCLK).

Chip Select (CS#)

When this input signal is High, the device is deselected and Serial Data Output Pinsare at high impedance. Unless an internal Program, Erase or Write Status Register cycle is in progress, the device will be in the Standby mode (this is not the Deep Power-down mode). Driving Chip Select (CS#) Low enables the device, placing it in the active power mode.

After Power-up, a falling edge on Chip Select (CS#) is required prior to the start of any instruction.

Hold (HOLD#) – SIO3

The Hold (HOLD#) signal is used to pause any serial communications with the device without deselecting the device.

During the Hold condition, the Serial Data Output (SO) is high impedance, and Serial Data Input (SI) and Serial Clock (SCLK) are Don't Care.

To start the Hold condition, the device must be selected, with Chip Select (CS#) driven Low.
Also, When the QE bit of Status Register is set for "High", the Hold# function is not available and this pin used for SIO3 in Quad mode.

Write Protect (WP#) – SIO2

The main purpose of this input signal is to freeze the size of the area of memory that is protected against program or erase instructions (as specified by the values in theBP2, BP1 and BP0 bits of the Status Register).
Like the Hold# pin, When the QE bit of Status Register is set for "High", the W# function is not available too, and this pin used for SIO2 in Quad mode.

4 Device Operation

4.1 SPI modes

SPI NAND supports two SPI modes

- CPOL=0, CPHA=0 (Mode 0)
- CPOL=1, CPHA=1 (Mode 3)

Input data is latched on the rising edge of SCLK and data shifts on the falling edge of SCLK for both modes. See Figure 4-1 for more details.

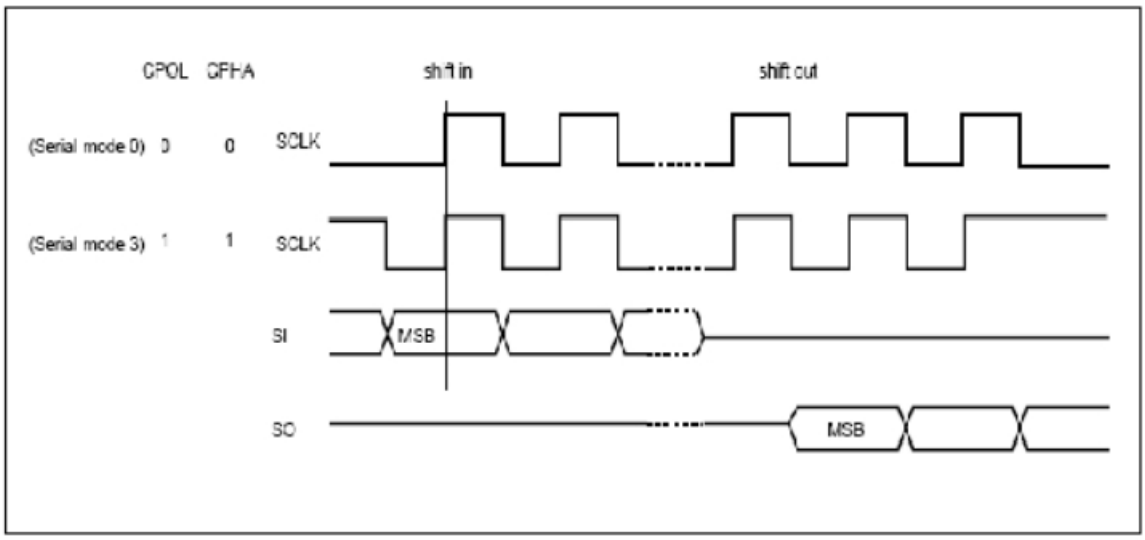


Figure 4-1 SPI Modes Sequence Diagram

Standard SPI

SPI NAND Flash supports four signal bus: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO).

Dual SPI

SPI NAND supports Dual SPI operation when using IO X2 and Dual IO instructions. When using Dual SPI instructions, the DI and DO pins become bidirectional IO (SIO0 AND SIO1) pins so that data are transferred at two times the rates of the standard SPI.

Quad SPI

SPI NAND supports Quad SPI operation when using IO X4 or Dual IO instructions. When using Quad SPI instructions, the DI, DO, WP#, HOLD# pins become bidirectional IO (SIO0, SIO1, SIO2, SIO3) so that data are transferred four times the rate of the standard SPI.

4.2 Hold Mode

When the HOLD# signal is low, the serial communications stop temporarily but the writing in the register, programming and erasing will continue.

To initiate a HOLD mode: CS is low. The HOLD mode will activate on the falling edge of the HOLD signal if the SCLK signal is already low.

To terminate HOLD mode: CS is low, and on the rising edge of the HOLD signal if the SCLK signal is already low.

During a HOLD mode, the SO is in high-impedance, and SI and SCLK are ignored.

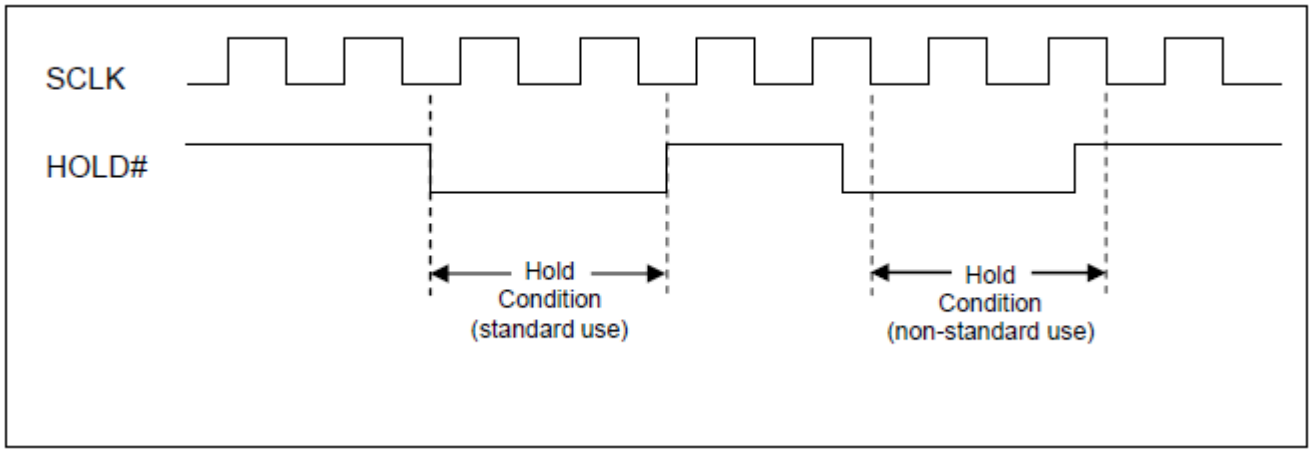


Figure 4-2 Hold Mode Sequence Diagram

4.3 Write Protection

SPI NAND provide write protection via both hardware and software. The WP# prevents the bits (BP0, BP1, BP2 and INV, CMP) from being accidentally altered. If BRWD = 1 & WP = 0, the BP0, BP1, BP2 and INV, CMP bits will not be altered by any software. For more details, see “13.5 Block Protection”.

5. Command Set

Table 5-1 Commands Set

Command Name	Byte1	Byte2	Byte3	Byte4	Byte5	ByteN
Write Enable	06H					
Write Disable	04H					
Get Features	0FH	A7-A0	(D7-D0)			Wrap
Set Feature	1FH	A7-A0	(D7-D0)	Dummy		
Page Read(to cache)	13H	A23-A16	A15-A8	A7-A0		
Read form Cache	03H/0BH	A15-A8	A7-A0	dummy	(D7-D0)	Wrap
Read form Cache x 2	3BH	A15-A8	A7-A0	dummy	(D7-D0)x2	Wrap
Read form Cache x 4	6BH	A15-A8	A7-A0	dummy	(D7-D0)x4	Wrap
Read form Cache Dual IO	BBH	A15-A0	dummy	(D7-D0)x2		Wrap
Read form Cache Quad IO	EBH	A15-A0	(D7-D0)x4			Wrap
Read ID	9FH	A7-A0	MID	DID		Wrap
Program Load	02H	A15-A8	A7-A0	(D7-D0)	Next byte	Byte N
Program Load x 4	32H	A15-A8	A7-A0	(D7-D0)x4	Next byte	Byte N
Program Execute	10H	A23-A16	A15-A8	A7-A0		
Program Load random data	84H	A15-A8	A7-A0	(D7-D0)	Next byte	Byte N
Program Load random data x 4	C4H/34H	A15-A8	A7-A0	(D7-D0)x4	Next byte	Byte N
Program Load random data Quad IO	72H	A15-A0	(D7-D0)x4	Next byte		Byte N
Block Erase	D8H	A23-A16	A15-A8	A7-A0		
Reset	FFH					

6 RESET Operations

RESET (FFh)

The RESET command (FFh) is used to put the memory device into a known condition and to abort the command sequence in progress. READ, PROGRAM, and ERASE commands can be aborted while the device is in the busy state. Once the RESET command is issued to the device, it will take tPOR to reset. During this period, the GET FEATURE command could be issued to monitor the status (OIP) except for 1Gb stacked device.

For 1Gb stacked device, no command should be issued until tPOR. The contents of the memory location being programmed or the block being erased are no longer valid. The first page data of the first block is auto-loaded to the cache register.

P_FAIL, E_FAIL, WEL, ECCS1, and ECCS0 will be reset after the Reset (FFH) command is received. (Optional) The data of Block 0 Page 0 will be automatically loaded to cache after the RESET (FFH) command is received, and ECCS1 and ECCS0 will show BCH results.

The command sequence is described as follows.

FFH (RESET)

0FH (GET FEATURE)

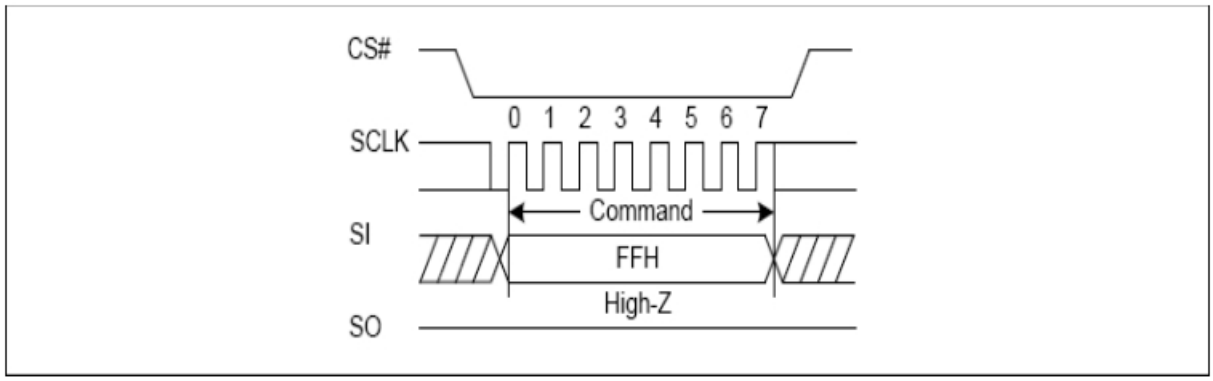


Figure 6-2 Reset Sequence Diagram

Notes:

1. Users should use RESET (FFH) command and GET FEATURE (0FH) command after power-up to confirm that the system is initialized (Block 0 Page 0 are loaded; the internal initialization finished). Otherwise, premature command accessing will lead to some unexpected results. If not to use the RESET (FFH) command, the device should not be operated until 5ms past powe-up.
2. Users should use the GET FEATURE (0FH) command after using the RESET (FFH) command to make sure that the interrupt operation is completed (OIP = 0) and finish the loading of Block 0 Page 0. Otherwise, it will result in some unexpected results.

7 Write Operation

7.1 Write Enable (WREN) (06h)

The Write Enable command (WREN) is used to enable WEL bit(set it to 1).The WEL bit must be set to 1 before using the following commands:

Page program

OTP program/OTP protection

Block erase

Notes:

1. WEL bit will be automatically cleared after executing the above commands.
2. WEL bit will be automatically cleared after receiving the RESET (FFH) command.

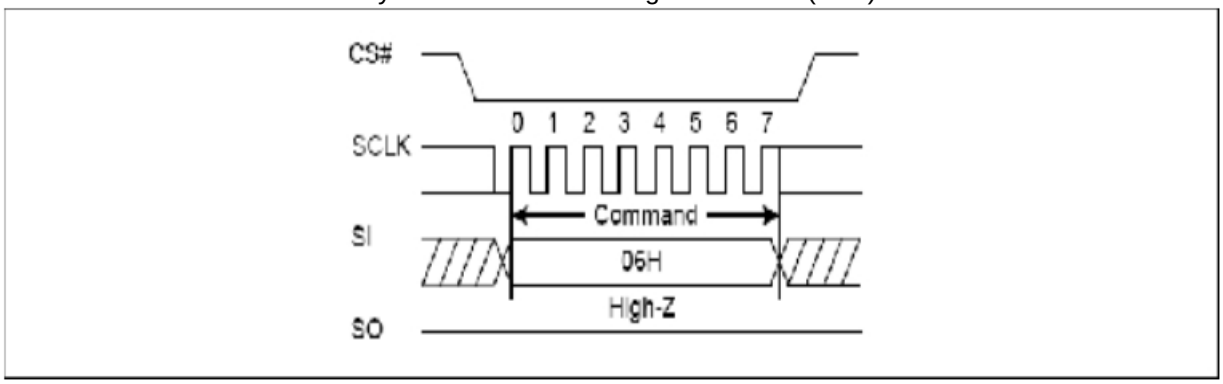


Figure 7-1 Write Enable Sequence Diagram

7.2 Write Disable (WRDI) (04h)

The Write Disable (WRDI) command is used to disable WEL(reset it to 0).

Notes: WEL will be automatically cleared after receiving the RESET (FF) command.

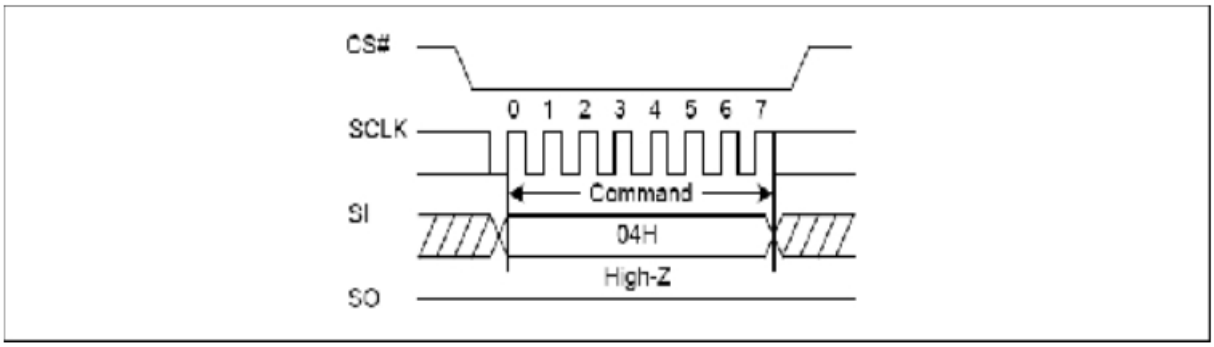


Figure 7-2 Write Disable Sequence Diagram

8 FEATURE OPERATIONS

8.1 Get Features (0Fh) & Set Features (1Fh)

The GET FEATURES (0FH) and SET FEATURES (1FH) commands are used to monitor and alter the working status of SPI NAND FLASH.

These commands use a 1-byte feature address to determine which feature is to be read or modified.

The features in the feature byte B0H are all volatile except OTP_PRT bit.

All registers have a default value after power-up (except the non-volatile bit).

P_FAIL, E_FAIL, and WEL will be cleared after the RESET (FF) command being executed, while other registers will not be impacted.

The value of all reserved bits is 0 (even after being set to 1).

Table 8-1 Features Settings

Register	Addr.	7	6	5	4	3	2	1	0
Protection	A0H	BRWD	reserved	BP2	BP1	BP0	INV	CMP	Reserved
Feature	B0H	OTP_PRT	OTP_EN	reserved	ECC_EN	reserved	reserved	reserved	QE
Status	C0H	Reserved	Reserved	ECCS1	ECCS0	P_FALL	E_FALL	WEL	OIP

Notes:

If BRWD is enabled and WP# is LOW, then the block lock register cannot be changed.

If QE is enabled, the quad IO operations can be executed.

All the reserved bits must be held low when the feature is set.

These registers are write/read type, except for Register of Status (C0H) is read only.

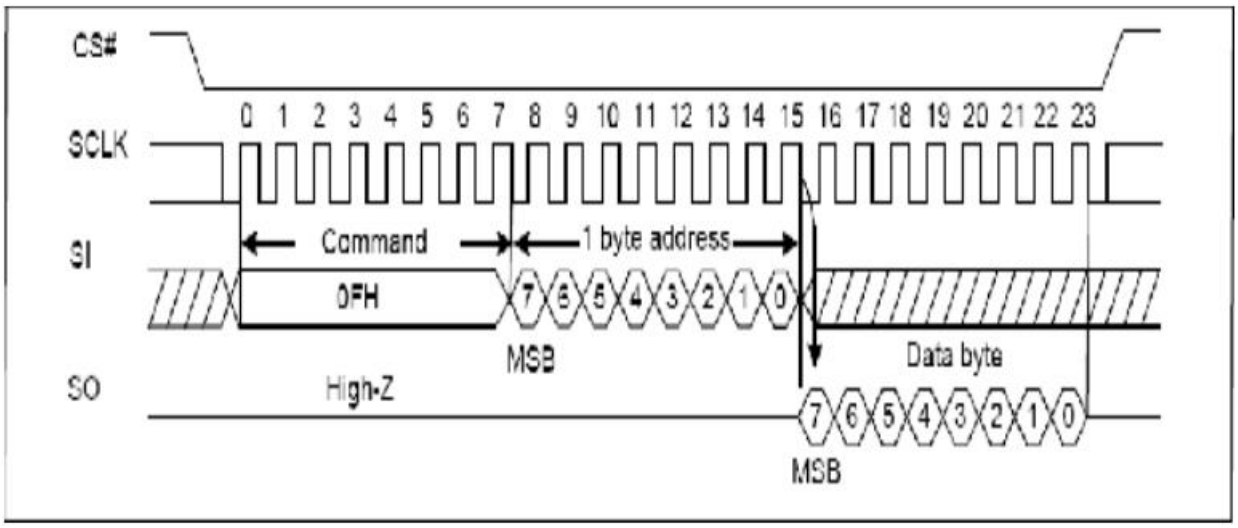


Figure 8-1 Get Features Sequence Diagram

Notes:

The output would be updated by real-time, until CS# is driven high.

The set features command supports a dummy byte mode after the data byte as well. The features in the feature byte B0H are all volatile except OTP_PRT bit.

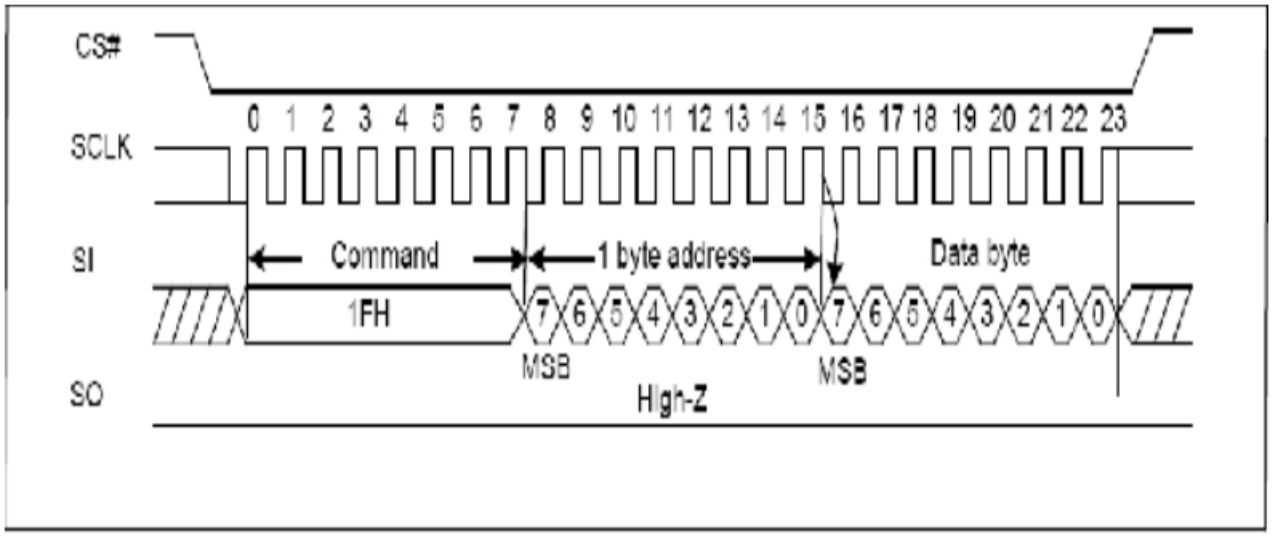


Figure 8-2 Set Features Sequence Diagram

9 READ ID (9Fh)

The READ ID command is used to identify the SPI NAND FLASH and reads a two-byte table that includes the Manufacturer ID and Device ID. Table 9-1 shows the address and description of the register. Figure 9-1 shows the command sequence

- Manufacturer identification (one byte)
- Device identification (one byte)

Table 9-2 READ ID Table

Address	Value	Description
00H	F2	Manufacturer ID
01H	0A	Device ID

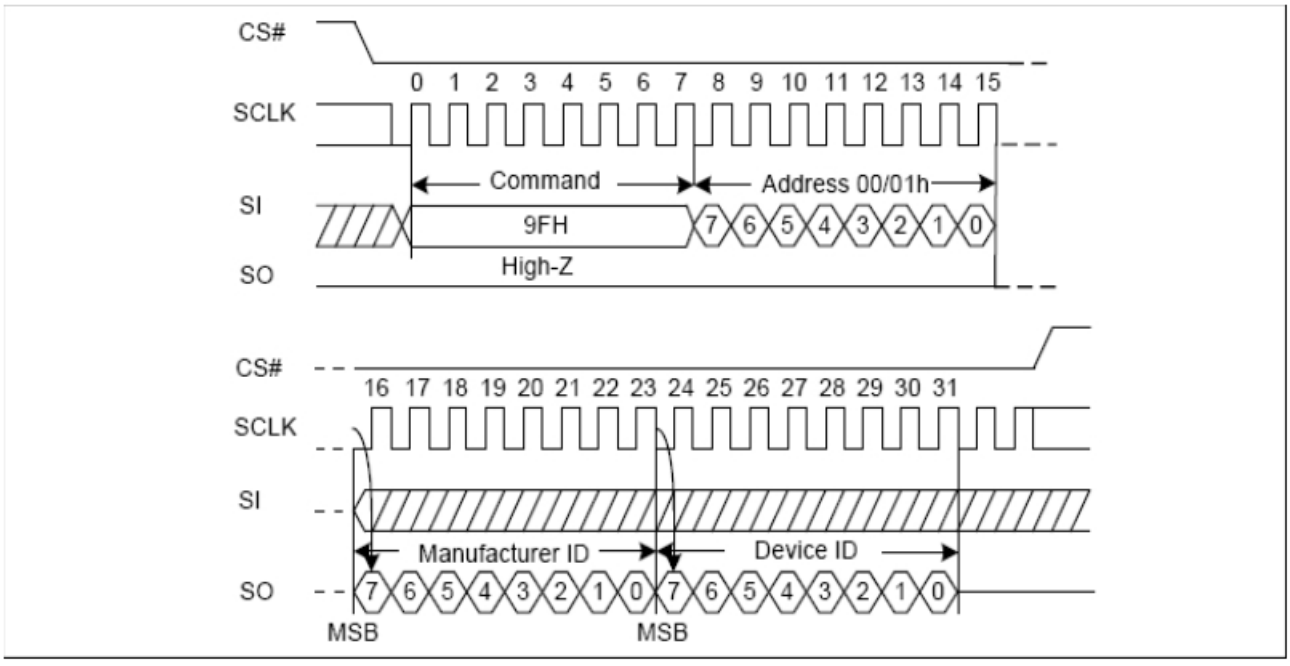


Figure 9-1 Read ID Sequence Diagram

10 READ OPERATIONS

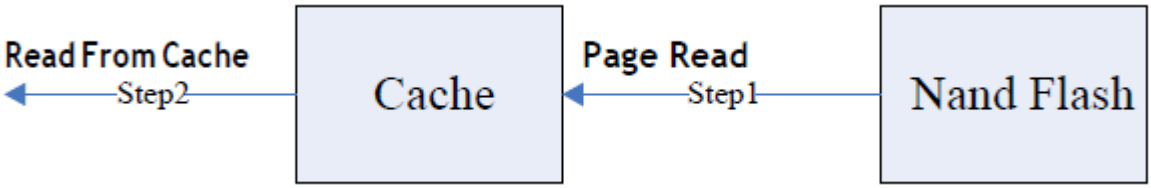


Figure 10-1 Page Read Operations Diagram

It takes three steps to read data from the SPI NAND Flash:

1 Use PAGE READ (13H) command to load the data page to the Cache.

2 Use GET FEATURES (0FH) command to check the status register (C0H). The OIP bit in status register will be HIGH until the loading operation is finished. Users may also read ECCS1 and ECCS0 to check if the data acquired is correct if ECC_EN is enabled.

3 Use READ FROM CACHE (03H/0BH/3BH/6BH/BBH/EBH) command to read the data page from the Cache.

The address (16 bits) of the READ FROM CACHE command contains 4-bit wrap address to indicate three kinds of wrap modes and 12-bit column address to designate the starting byte address of cache. The starting byte address must be within 0 to 2111. After the end of the cache register is reached, the data wraps around the beginning boundary automatically until CS# is pulled high to terminate this operation.

Table 10-1 Wrap configure bit table

Wrap<3>	Wrap<2>	Wrap<1>	Wrap<0>	Wrap Length(byte)
0	0	X	X	2112
0	1	X	X	2048
1	0	X	X	64
1	1	X	X	16

10.1 Page Read to Cache (13h)

The PAGE READ (13H) command is used for NAND FALSH to read data and load them to the Cache (If ECC_EN is enabled, the data will be decoded in BCH before being loaded to the Cache). The address should be 24-bit, and the length of the Page / Block address depends on the specifications of the Flash (refer to Figure 2-2). After successfully mapping, SPI NAND FLASH will load the corresponding NAND FLASH data to the Cache. tRD represents the load time. In this process, users may use GET FEATURE (0FH) command to check the OIP (“OIP = 0” means the loading operation is finished). Then, use the READ FROM CACHE (03H/0BH/3BH/6BH/BBH/EBH) command to read the data from the Cache

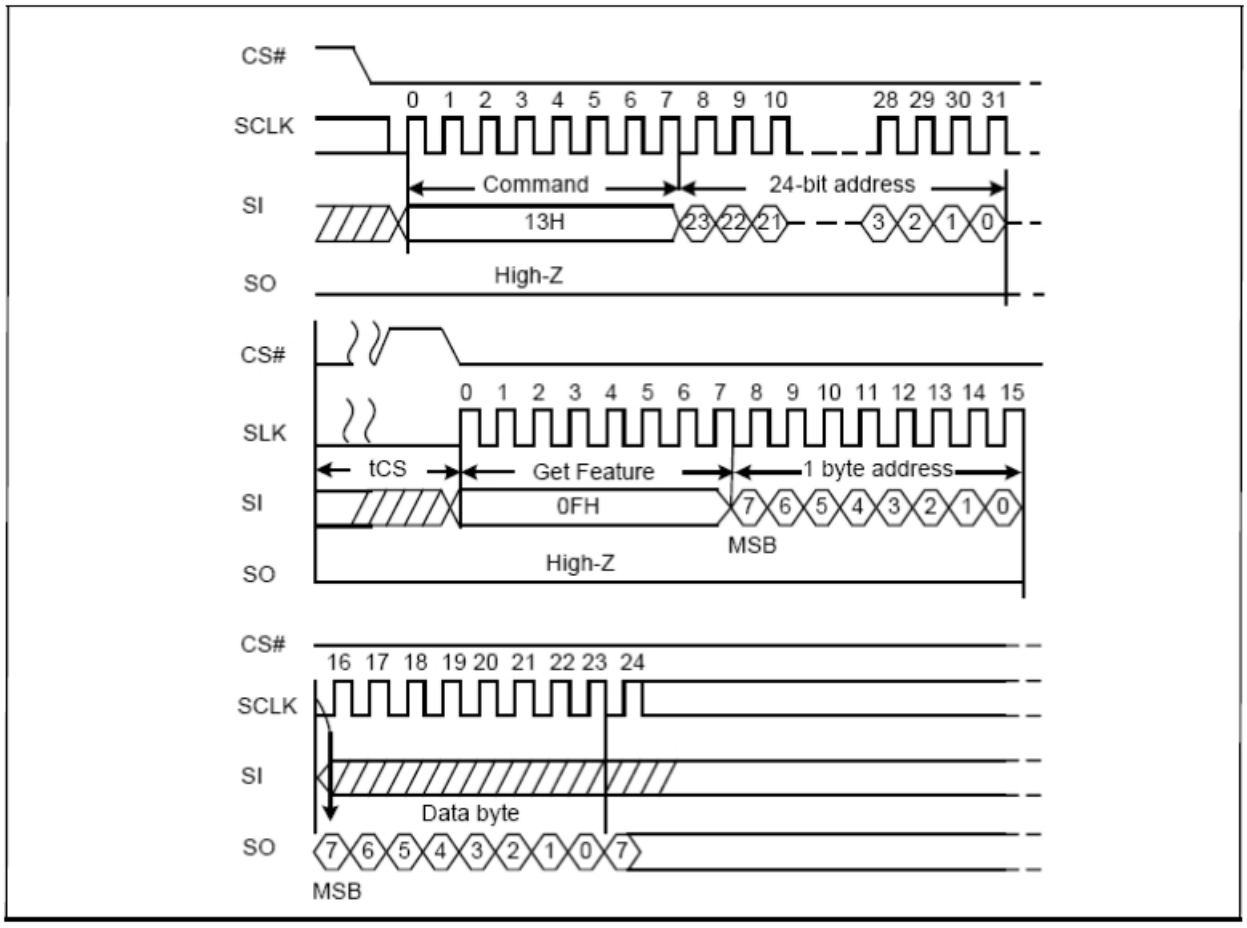


Figure 10-2 Page Read to cache Sequence Diagram

10.2 Read From Cache (03h or 0Bh)

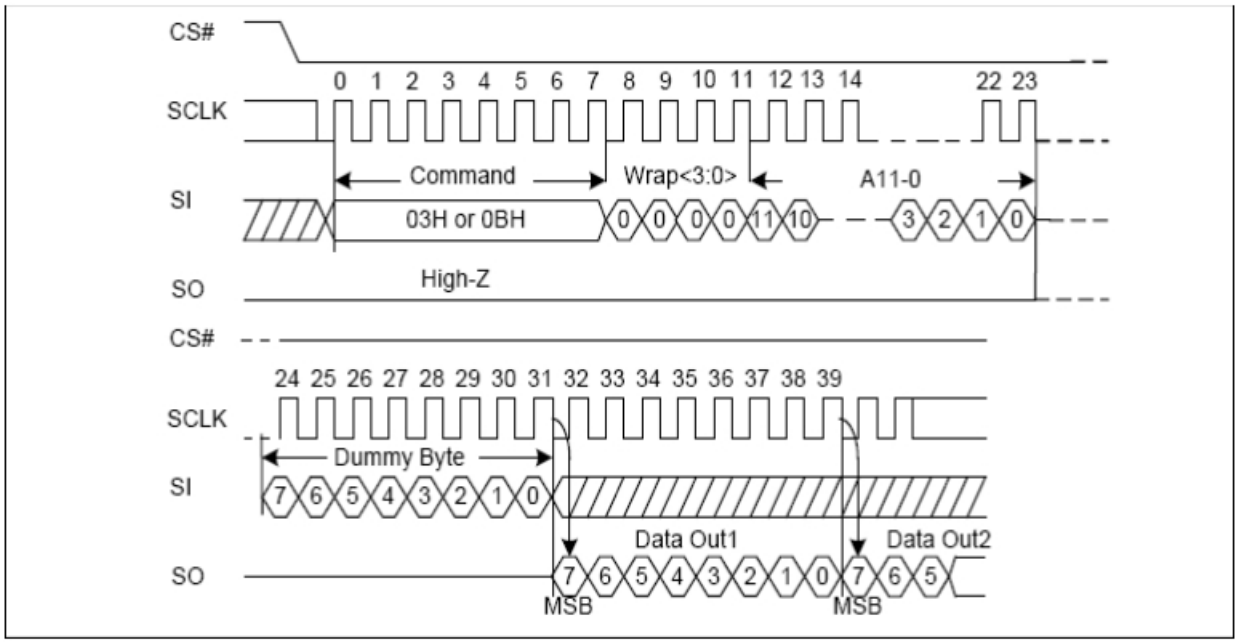


Figure 10-3 Read From Cache Sequence Diagram

10.3 Read From Cache x2 (3Bh)

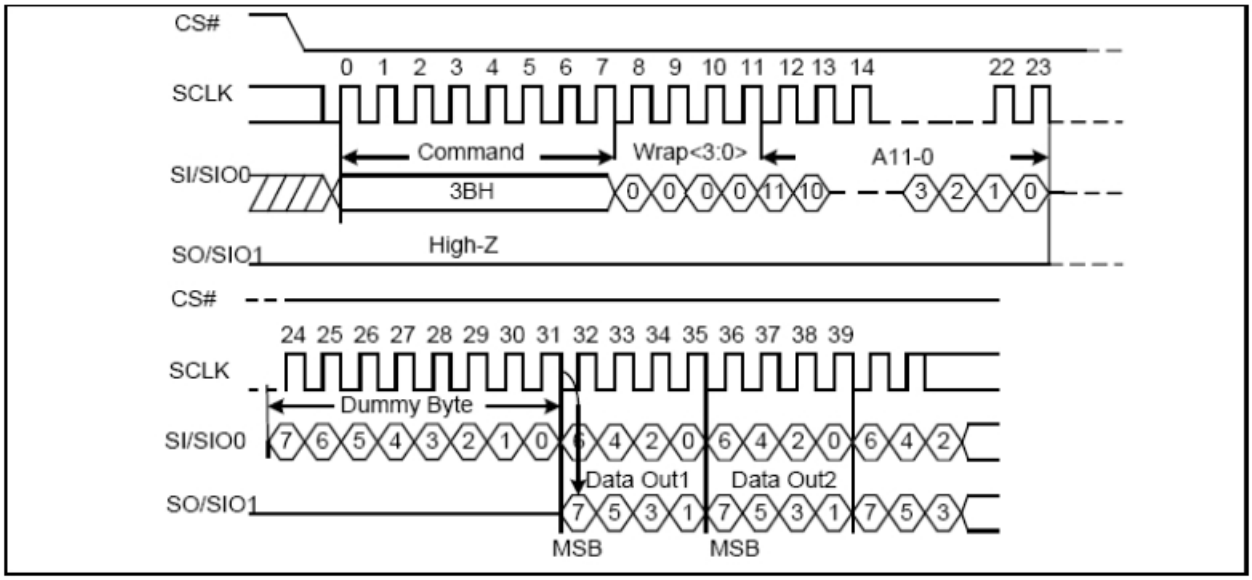


Figure 10-4 Read From Cache x2 Sequence Diagram

10.4 Read From Cache x4 (6Bh)

The QE bit must be set to 1 before using the Read From Cache x4 command

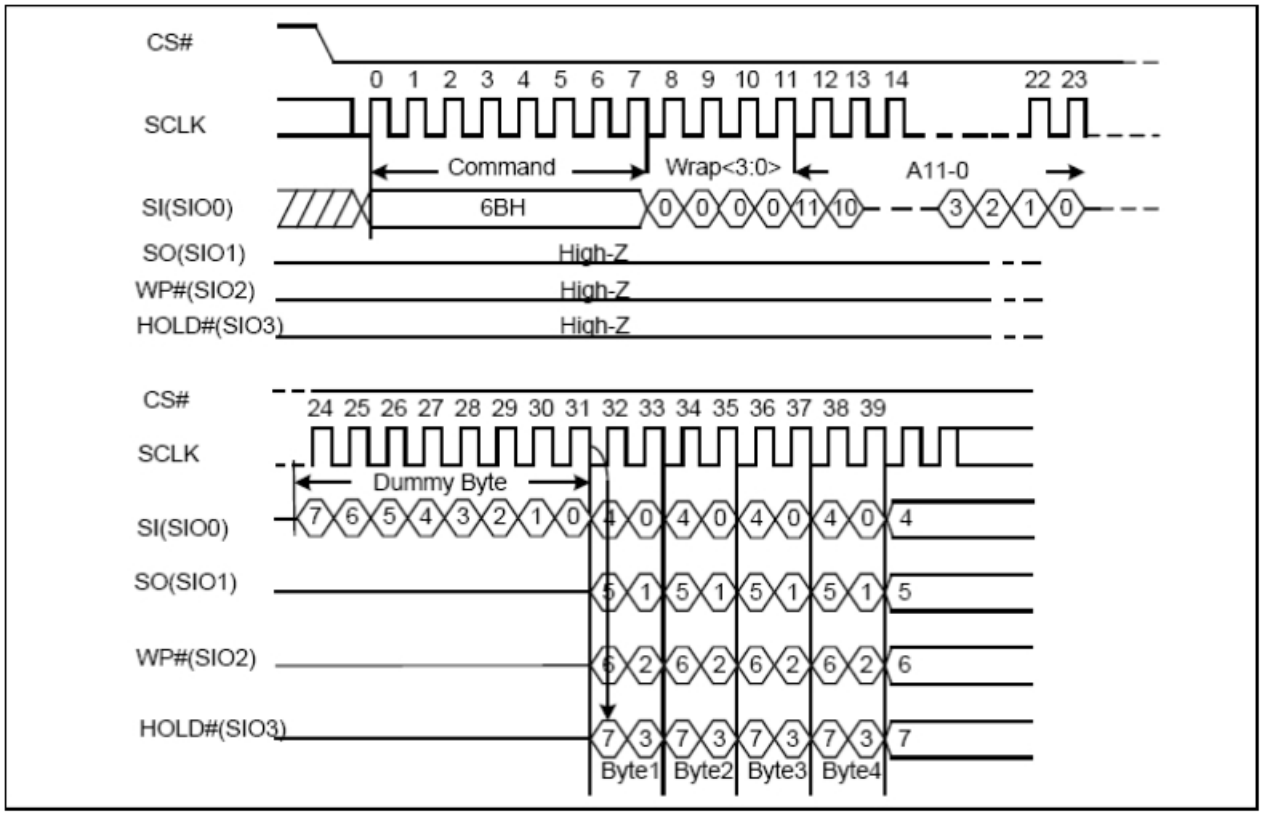


Figure 10-5 Read From Cache x4 Sequence Diagram

10.5 Read From Cache Dual I/O (BBh)

The Read From Cache Dual I/O demand (BBH) is similar to Read From Cache x2 command (3BH), but the address fields (wrap<3:0> A11-0) are transmitted by SIO0 and SIO1.

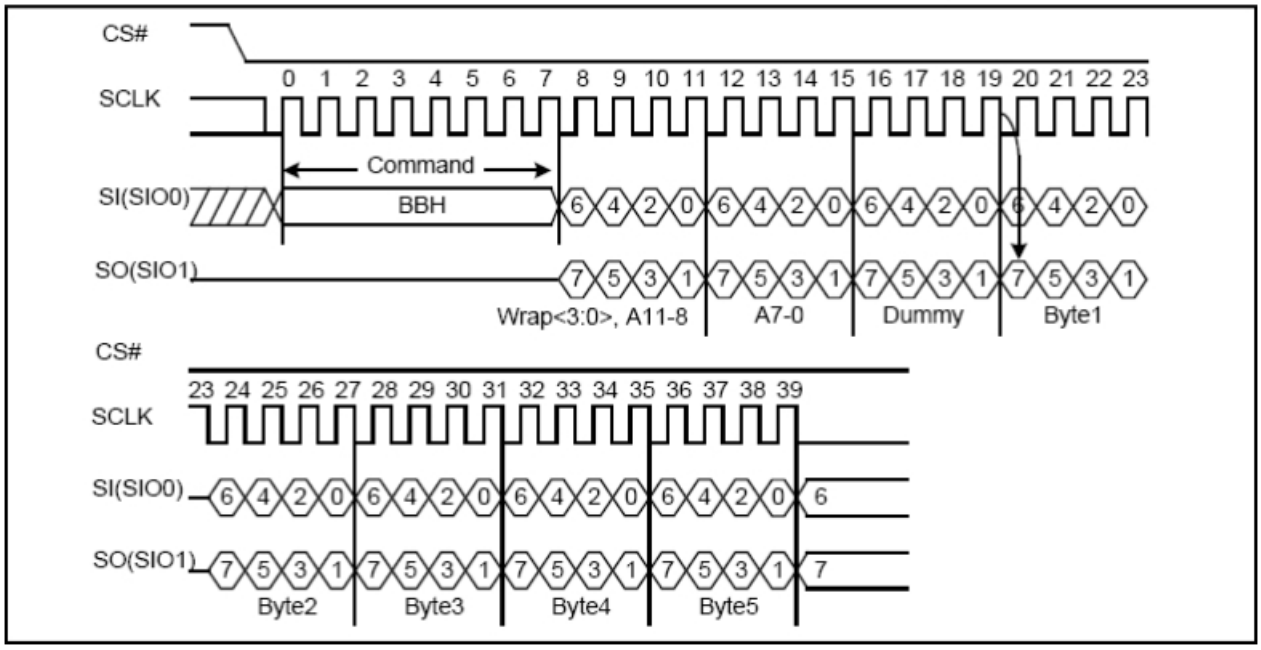


Figure 10-6 Read From Cache Dual IO Sequence Diagram

10.6 Read From Cache Quad I/O (EBh)

The Read From Cache Quad IO Dual I/O command (EBH) is similar to Read From Cache x4 command (6BH), but the address fields (wrap<3:0> A11-0) are transmitted by SIO0, SIO1, SIO2 and SIO3. Before using this command, the QE bit must be set to 1

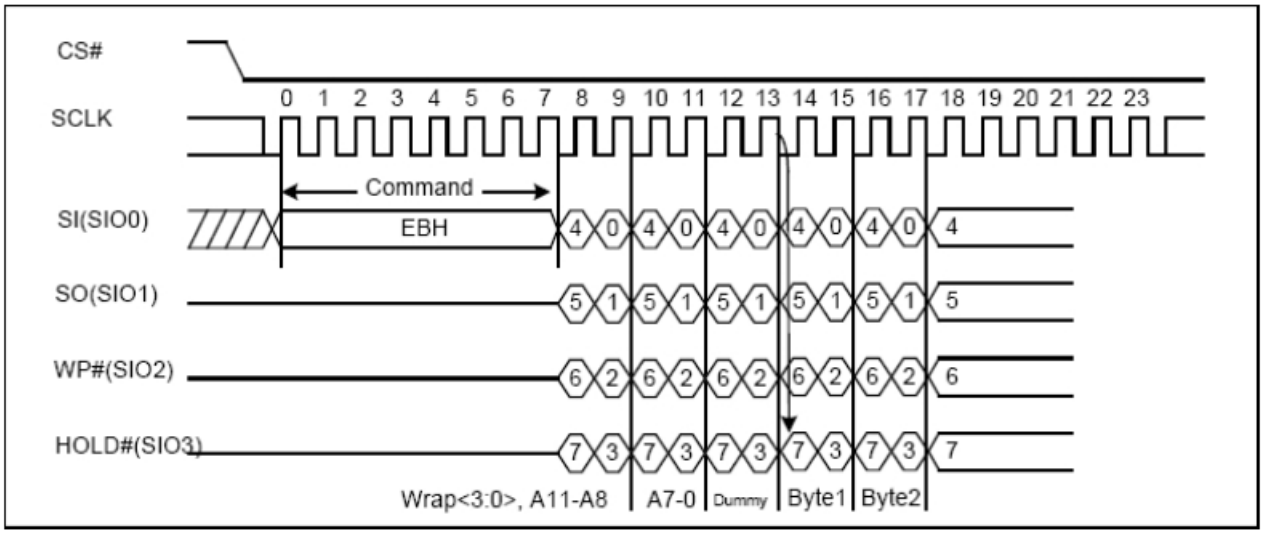


Figure 10-7 Read From Cache Quad IO Sequence Diagram

11 Page Program Operations

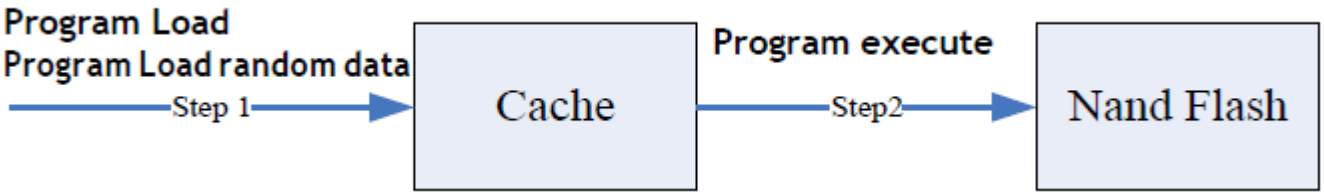


Figure 11-1 Page Program Operations Diagram

It takes four steps to write data to the SPI NAND Flash:

1. Use the PROGRAM LOAD (02H/32H) command or PROGRAM LOAD RANDOM DATA (84H/C4H/ 34H/72H) command to load the data page to the Cache;
2. WRITE ENABLE (06H);
3. Use the PROGRAM EXECUTE (10H) command to program the data page into the NAND FLASH.

4 Use the GET FEATURES (0FH) command to check the status register (C0H) until the program operation is accomplished (OIP = 0). Check P_FAIL to make sure if the program operation is successful or not("P_FAIL= 0" means success).

According to different program requirements, the specific commands sequence used are as follows

11.1 Program Load & Page Program

The PROGRAM LOAD is used to program 1-to-2112-byte data into the NAND FLASH and the commands sequence are as follows:

02H (PROGRAM LOAD) /32H (PROGRAM LOAD x4)

06H (WRITE ENABLE)

10H (PROGRAM EXECUTE)

0FH (GET FEATURE)

The address of the PROGRAM LOAD (02H/32H) command contains 4 dummy bits and 12-bit column address. It is used to load data into the Cache. If more than 2112 bytes are loaded, the additional bytes will be ignored. Issue the WRITE ENABLE (06H) command to set WEL to 1. If WEL = 0, the subsequent program operation will be ignored and P_FAIL=0. Then use the PROGRAM EXECUTE (10H) command to write the data in the Cache into the NAND FLASH. Use GET FEATURE (0FH) command to check the program result. "OIP = 0" means the program operation is completed, and "P_FAIL= 0" means the operation is successful. If P_FAIL=1, the program operation fails and the user can refer to the description of P_FAIL in the status register for detailed causes.

11.2 Internal data Move & Page Program

PROGRAM LOAD RANDOM DATA is used to alter portion or all of the data in the cache. Similar to the “Copy back” operation in NAND FLASH, the command sequence used are as follows:

13H (PAGE READ to cache)

84H/C4H/ 34H (PROGRAM LOAD RANDOM DATA)

84H/C4H/ 34H (PROGRAM LOAD RANDOM DATA)

06H (WRITE ENABLE)

10H (PROGRAM EXECUTE)

0FH (GET FEATURE)

Issue a PAGE READ (13H) command to read out the NAND FLASH page data that need altering into the cache and then issue a PROGRAM LOAD RANDOM DATA (84H/C4H/72H) command to update bytes of data in the page. Use WRITE ENABLE (06H) demand to set WEL to 1 and enable write. If WEL = 0, the subsequent programming will be ignored. Then issue a PROGRAM EXECUTE (10H) command to program the data in the Cache into the NAND FLASH. Use a GET FEATURE (0FH) command to check the program result. “OIP = 0” means the program operation is completed, and “P_FAIL= 0” means the program is successful. If P_FAIL=1, the program fails and users can refer to the description of P_FAIL in the status register for detailed causes.

11.3 Program Excute (PE) (10h)

PROGRAM EXECUTE (10H) is used to program the data from the cache into the NAND FLASH. The address should be 24-bit, and the length of the Page / Block address depends on the specifications of the Flash (refer to Figure 2-2). After successfully mapping, the data in the cache begin to program. tRD means the transferring time. In this process, users may use the GET FEATURE (0FH) command to check the OIP ("OIP = 0" means the operation is finished).

Data should be loaded into the cache before using the PROGRAM EXECUTE (10H) command, and there are two ways to load cache data: Program Load and Program Load Random Data.

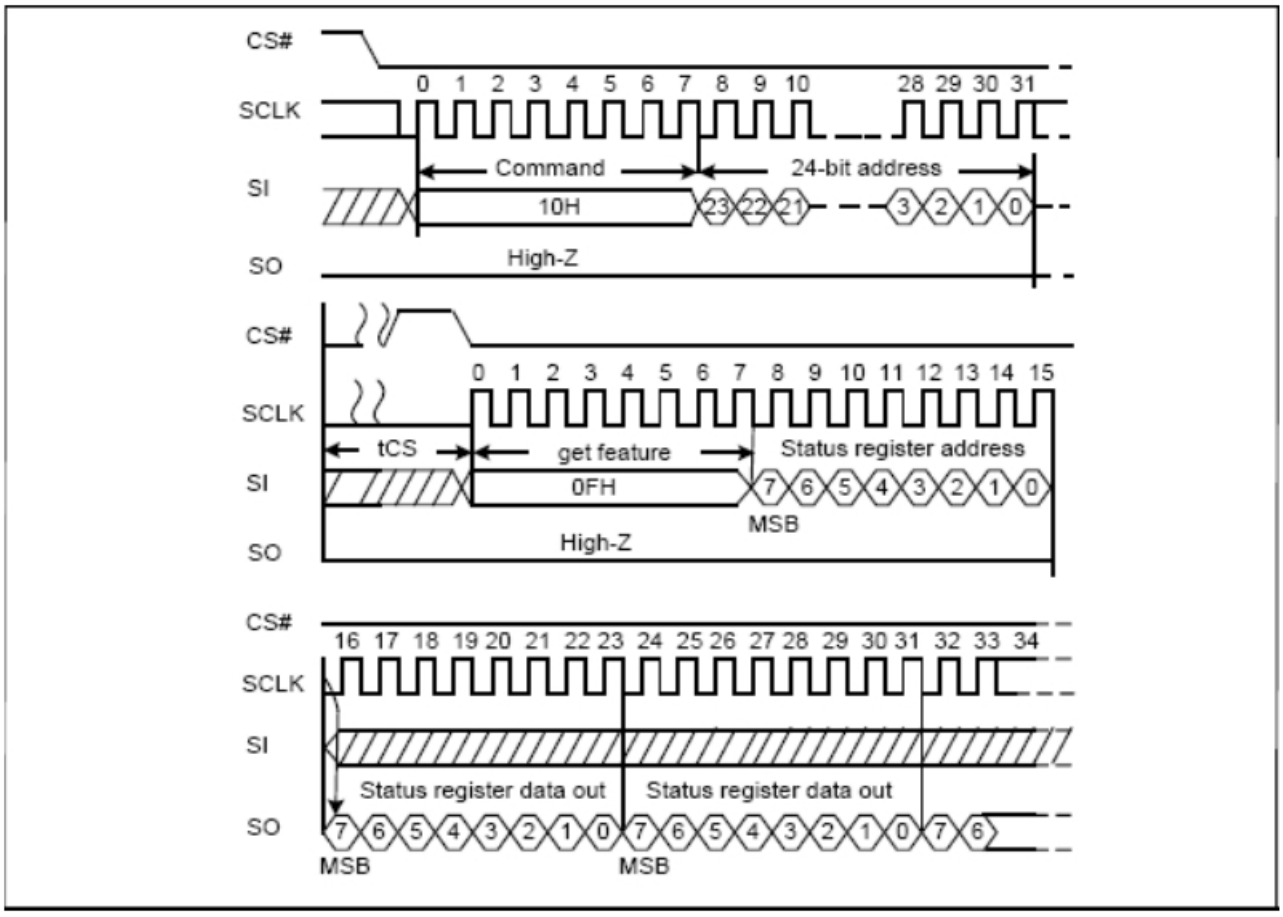


Figure 11-2 Program Execute Sequence Diagram

11.4 Program Load(PL) (02h)

The PROGRAM LOAD (02H) command address contains 4 dummy bits and 12-bit column address. The 12-bit column address is used to locate the starting byte address. If more than 2112 bytes are loaded, the additional bytes will be ignored. The CS# should not be set to high during the data transfer process or the transfer process will be forced to terminate.

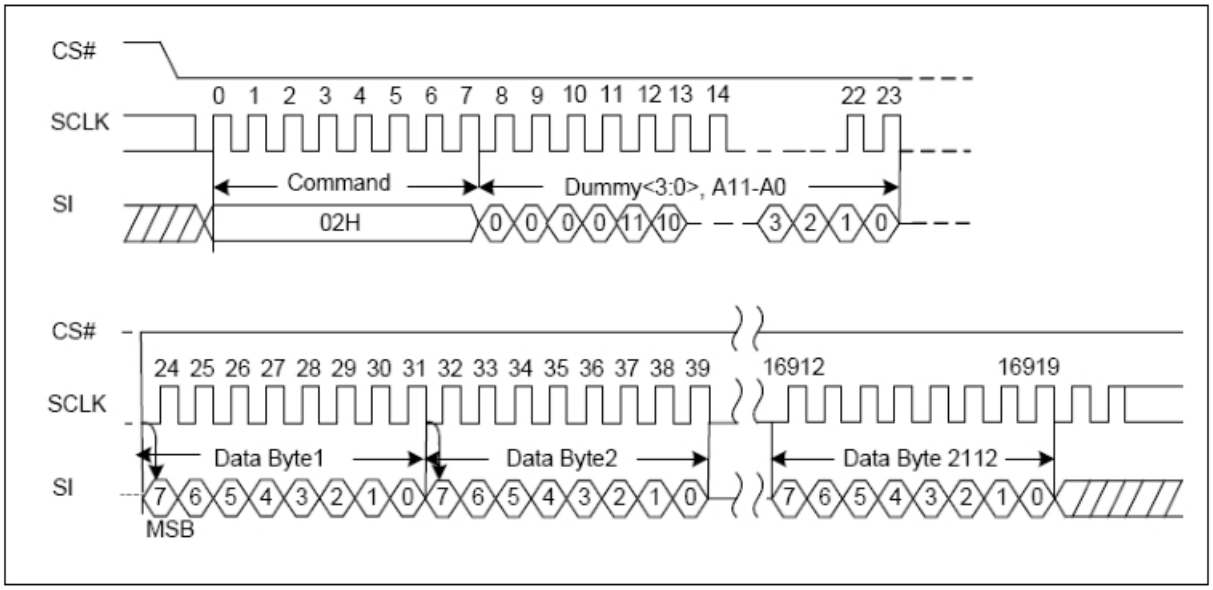


Figure 11-3 Program Load Sequence Diagram

11.5 Program Load x4 (PL x4) (32h)

The PROGRAM LOAD x4 (32H) command address contains 4 dummy bits and 12-bit column address. The 12-bit column address is used to locate the starting byte address. The QE bit must be set to 1 before using the Program Load x4 command. If more than 2112 bytes are loaded, the additional bytes will be ignored. The CS# should not be set to high during the transfer process or the transfer process will be forced to terminate.

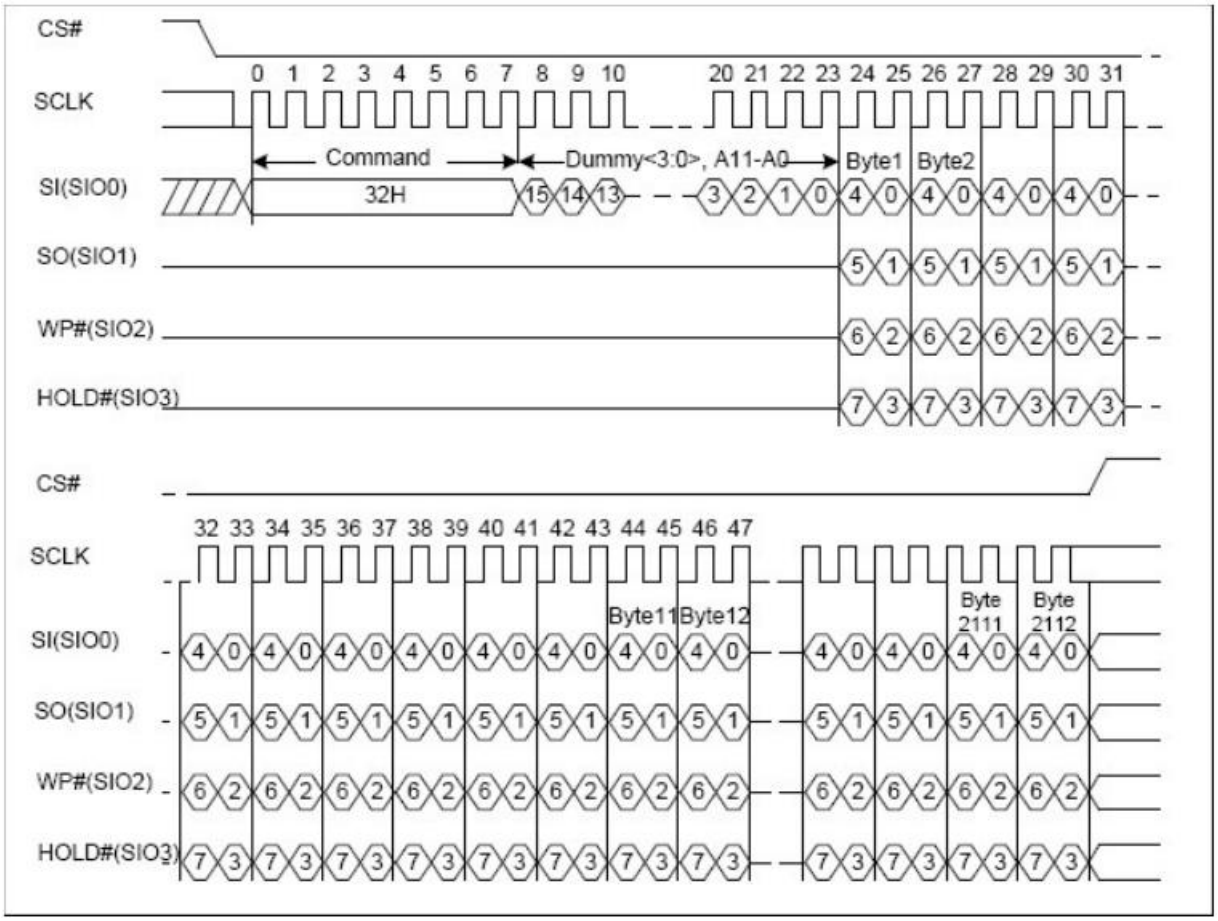


Figure 11-4 Program Load x4 Sequence Diagram

11.6 Program Load Random Data (84h)

The PROGRAM LOAD RANDOM DATA (84H) command contains 4 dummy bits and 12-bit column address. The 12-bit column address is used to locate the starting byte address. If more than 2112 bytes are loaded, the additional bytes will be ignored. The CS# should not be set to high during the transfer process or the transfer process will be forced to terminate.

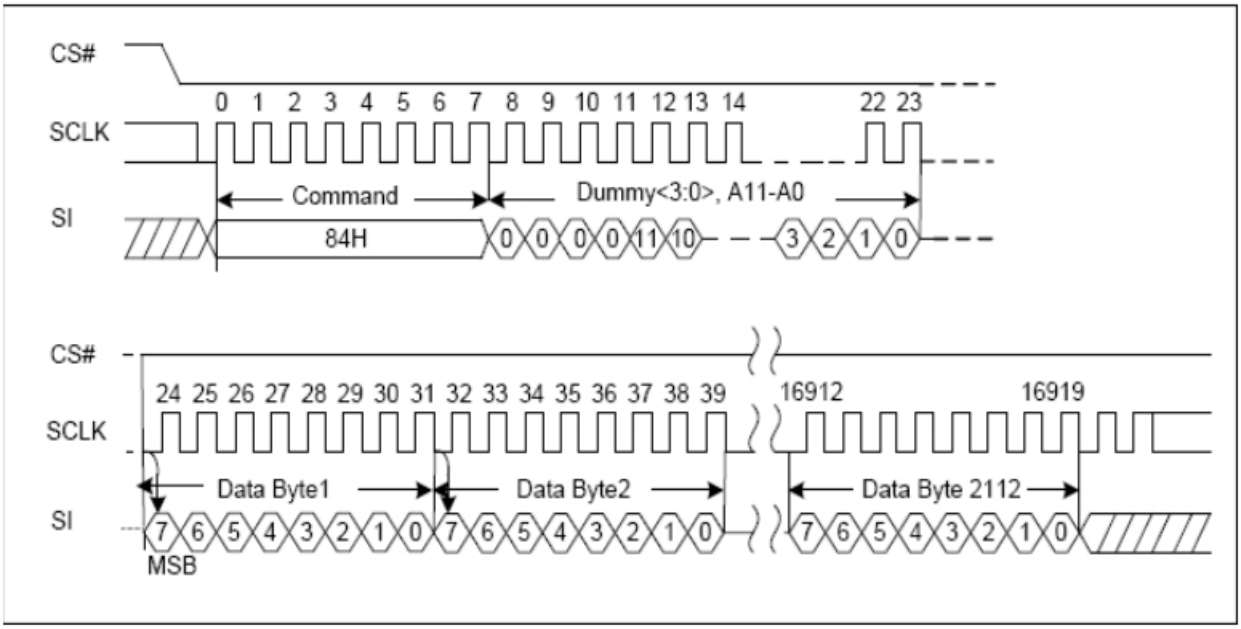


Figure 11-5 Program Load Random Data Sequence Diagram

11.7 Program Load Random data x4 (C4h/34h)

The PROGRAM LOAD RANDOM DATA x4 (C4H/34H) command contains 4 dummy bits and 12-bit column address. The 12-bit column address is used to locate the starting byte address. If more than 2112 bytes are loaded, the additional bytes will be ignored. The CS# should not be set to high during the transfer process or the transfer process will be forced to terminate. The QE bit must be set to 1 before using the command.

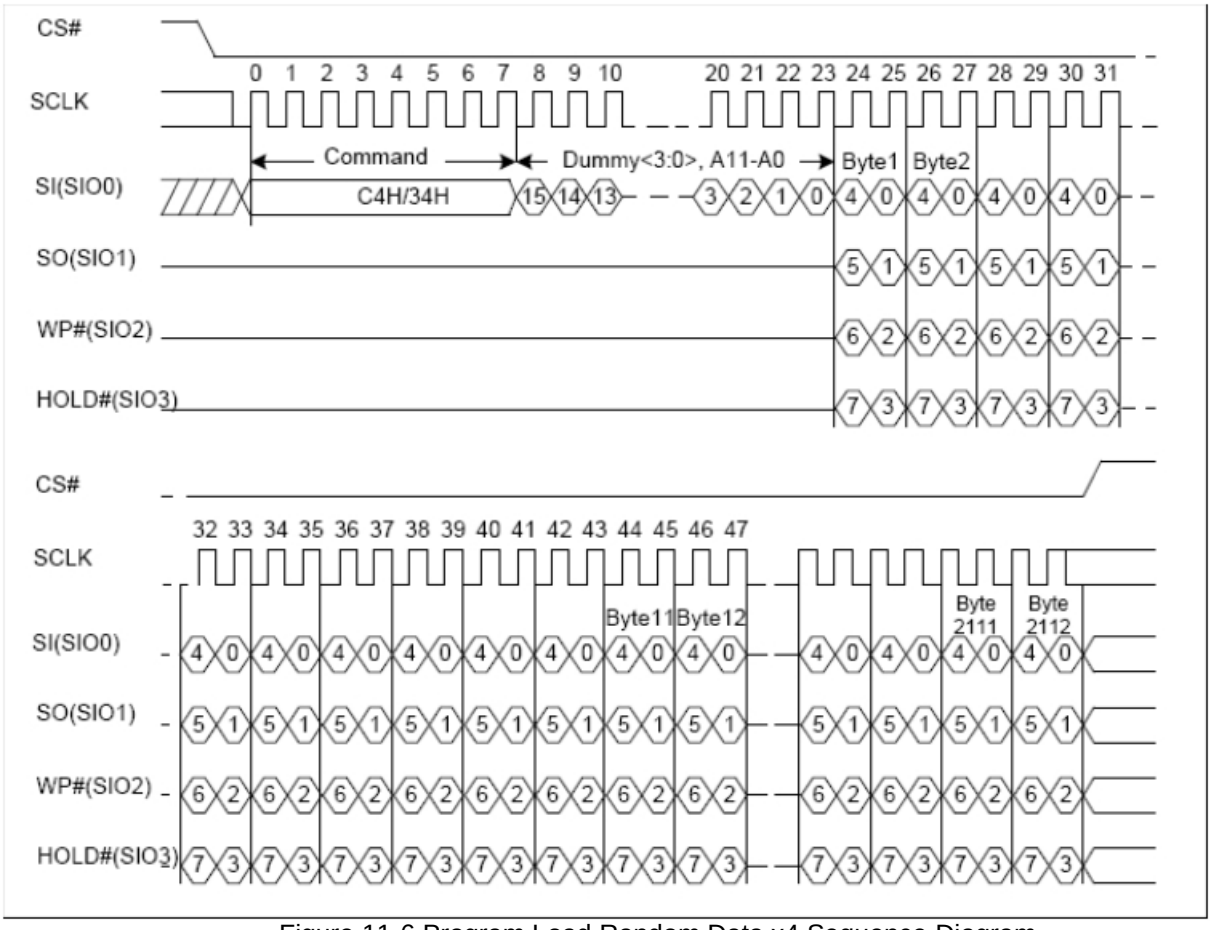


Figure 11-6 Program Load Random Data x4 Sequence Diagram

11.8 Program Load Random data Quad I/O (72h)

The Program Load Random Data Quad IO (EBH) command is similar to the PROGRAM LOAD RANDOM DATA x4(C4H/34H) command, but the address fields (dummy<3:0> A11-0) are transmitted by SIO0, SIO1, SIO2, and SIO3. The QE must be set to 1 before using the command. If more than 2112 bytes are loaded, the additional bytes will be ignored. The CS# should not be set to high during the transfer process or the transfer process will be forced to terminate

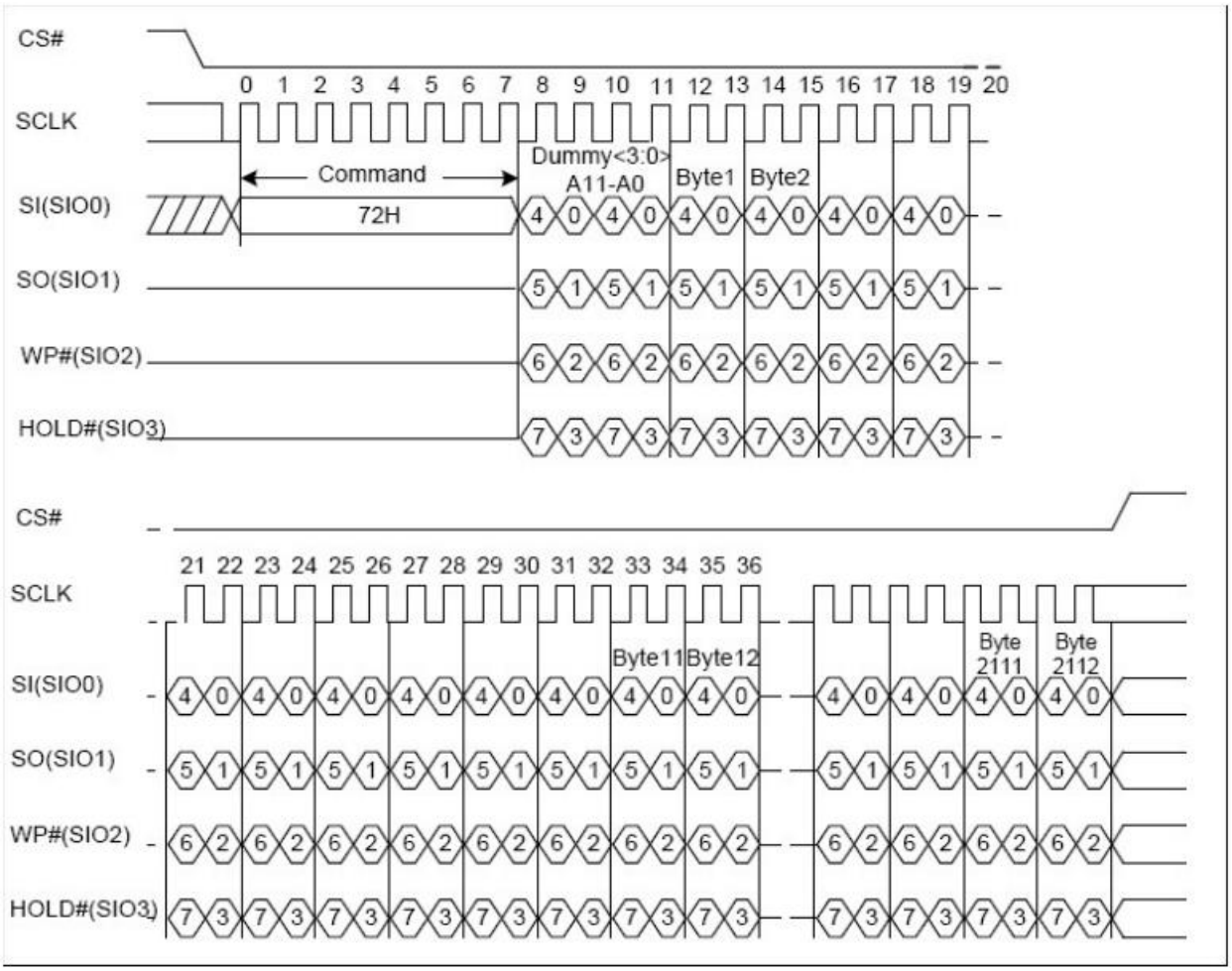
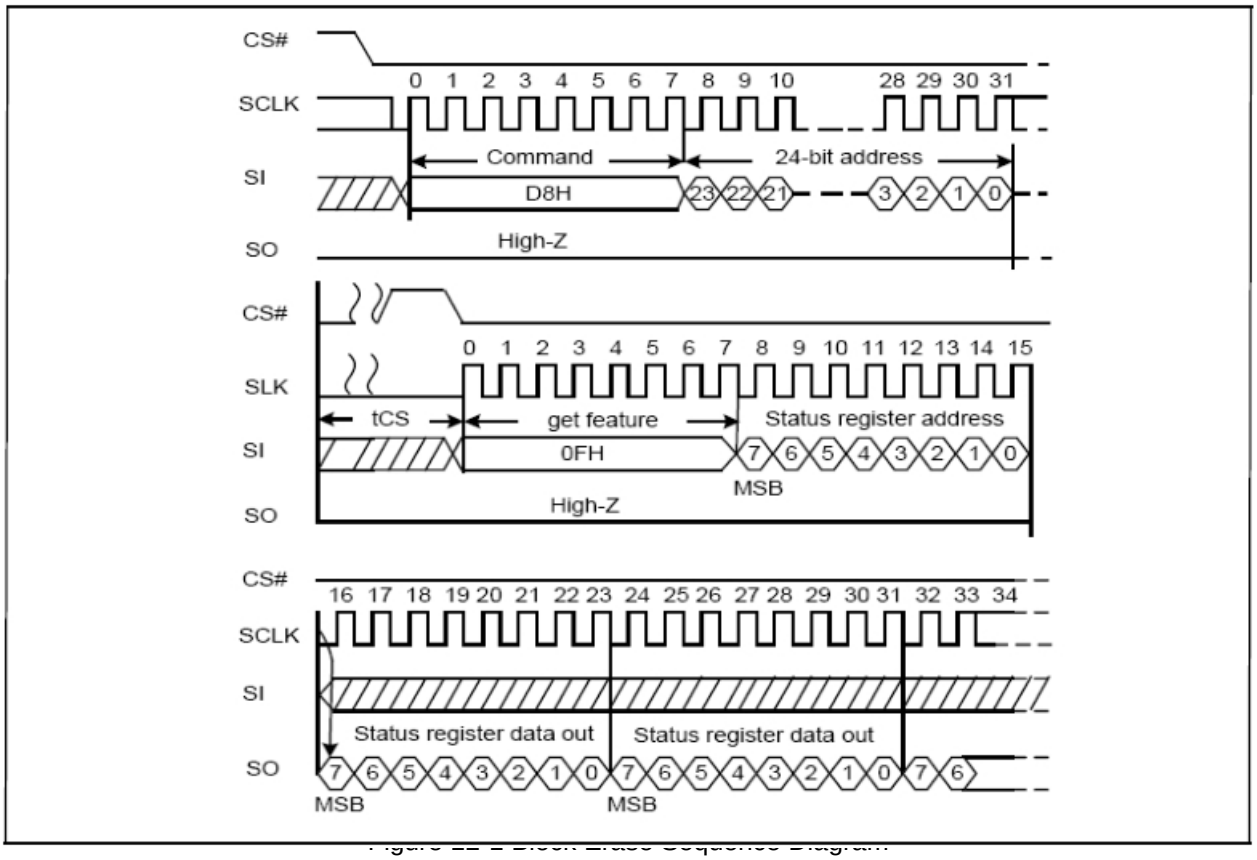


Figure 11-7 Program Load Random Data Quad IO Sequence Diagram

12 ERASE OPERATIONS

12.1 Block Erase (D8h)



The BLOCK ERASE (D8H) command is used to erase the NAND FLASH block. The address of this command is 24-bit, and the length of the Page / Block address depends on the specifications of the Flash (refer to Figure 2-2). After successfully mapping, the erase operation begins. tERS means the busy time of erase process. In this process, users may issue a GET FEATURE (0FH) command to check the OIP and monitor the erase results. “OIP = 0” means the erase operation is finished, and “E_FAIL= 0” means the operation is successful. If E_FAIL = 1, the operation fails and users can refer to the description of P_FAIL in the status register for detailed causes.◦

While a BLOCK ERASE (D8H) command is in progress (OIP = 1), users can use a READ FROM CACHE command (03H/0BH/3BH/6BH/BBH/EBH) to read the cache or use a PROGRAM LOAD command (02H/32H/84H/C4H/ 34H/72H) to write the cache.

The commands sequence is as follows:

06H (WRITE ENABLE)
D8H (BLOCK ERASE)
0FH (GET FEATURE)

13 Functional Features

13.1 OTP Region

SPI NAND FLASH provides a special One-Time Programmable memory area. The OTP region size is four pages and each page is 2112-byte. Users can use this region any way they want, like programming serial numbers or storing backup data tables.

Table 13-1 Feature Register

Register	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Feature	B0H	OTP_PRT	OTP_EN	Reserved	ECC_EN	Reserved	Reserved	Reserved	QE
-	-	Non-volatile	Read & Write	-	Read & Write	-	-	-	Read & Write

When delivered from factory, the OTP_PRT bit is 0.To use the OTP, users should issue a SET FEATURES command to set the OTP_EN bit of the Feature Register. The PROGRAM LOAD (02H/32H) or PROGRAM RANDOM (84H/C4H/34H/72H) and PROGRAM EXECUTE (10H) commands can be used to program Page 00 to 03. Also, the PAGE READ (13H) and READ FROM CACHE (03H/0BH/3BH/6BH/BBH/EBH) commands can be used to read the OTP area. To lock the OTP region, users should first use the SET FEATURES command to set the OTP_EN bit and the OTP_PRT bit of the Feature Register and then use the PROGRAM EXECUTE (10H) command to finish locking.

Table 13-2 OTP States

OTP_PRT	OTP_EN	State
X	0	Normal operation; access the user's host storage.
0	1	Access the OTP region (read and program) Notes: **"OTP_PRT = 0"** means that the OTP is not locked yet. The OTP can be programmed many times, but the OTP pages that have been programmed cannot be programmed again, otherwise there will cause unexpected results.
1	1	1. When **OTP_PRT is 0**, users can set OTP_PRT and OTP_EN to 1 and then issue a PROGRAM_EXECUTE (10H) command to lock the OTP. After that, the OTP_PRT will permanently remain 1 (no matter the device is powered up or not). 2. When the OTP_PRT is 1, users can only read the OTP region.

Enter the OTP Mode

Issue a SET FEATURES (1FH) command

Feature register B0H

Set the OTP_EN bit to 1

Access the OTP Date

Issue a PAGE READ (13H) command after entering the OTP mode.

Issue a READ FROM CACHE command (03H/0BH/3BH/6BH/BBH/EBH) to read out data from the cache.

Write Data into OTP (only when OTP_PRT is 0)

Enter the OTP mode

Issue the WRITE ENABLE (06H) command

Use the PROGRAM LOAD (02H/32H) or PROGRAM RANDOM (84H/C4H/34H/72H) command to write data into the cache

Issue the PROGRAM EXECUTE (10H) command

- Use the GET FEATURES (OFH) command to check if the operation is finished (“OIP = 0” means it is finished, and “P_FAIL = 0” means it is successful)

Repeat step 2 and its subsequent steps and use the OTP address to program

Lock the OTP Region

Use SET FEATURES (1FH) command to set the OTP_EN and OTP_PRT bit

Issue the WRITE ENABLE (06H) command

Issue the PROGRAM EXECUTE (10H) command

After the OTP region is locked, the OTP_PRT bit will be forever 1 and the OTP region cannot be erased or programmed again.

13.2 Status Register

The SPI NAND FLASH has an 8-bit status register that software can read during the device operation for operation state query, such as the ECC results of read operations (ECCS1 and ECCS0), the program results (P_FAIL), and the end of operations (OIP).

This register can be read by issuing the GET FEATURES (OFH) command followed by the feature address (C0H).

Table 13-3 Status Register

Register	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Status	C0H	Reserved	Reserved	ECCS1	ECCS0	P_FAIL	E_FAIL	WEL	OIP
—	—	—	—	Read only	Read only	Read only	Read only	Read only	Read only

Table 13-4 Description of Status Register

Bit-field	Bit name	Description
P_FAIL	Program results	P_FAIL = 0: program OK P_FAIL = 1: program Fail **Notes: Possible causes for P_FAIL to be 1:** The user programs an invalid address; The user programs a locked and protected OTP region; The users programs a protected region (BP0, BP1, BP2，INV, CMP). **Notes: Causes for reset:** The bit is cleared during the PROGRAM EXECUTE command sequence; The bit is cleared after receiving a reset command (FFH).
E_FAIL	Erase results	E_FAIL = 0: erase OK E_FAIL = 1: erase fail **Notes: Possible causes for E_FAIL to be 1:** The user erases an invalid address; The user erases an OTP region; The user erases a protected region (BP0, BP1, BP2，INV, CMP). **Notes: Causes for reset:** The bit is cleared at the start of the BLOCK ERASE command sequence;. The bit is cleared after receiving a RESET(FFH) command.

Table 13-4 Description of Status Register (Continued)

Bit-field	Bit name	Description
WEL	Enable Write	This bit indicates the current status of the WRITE_ENABLE (WEL = 1), WRITE_DISABLE, and (WEL = 0) commands. WEL must be 1 before using the PROGRAM_EXECUTE (10H) and the BLOCK_RASE (D8H) commands. Otherwise, the execution of the commands is invalid.
OIP	Operation in Progress	OIP indicates if the PAGE_READ (13H), PROGRAM_EXECUTE (10H) and BLOCK_RASE (D8H) commands are in progress. When using the RESET (FFH) command after powering up, OIP indicates the current status of the internal initialization. When using the RESET (FFH) command during operation, OIP indicates the current status of the stopping operation. **Notes: "OIP = 0" means the operation is accomplished and "OIP = 1" means the operation is in progress.**
ECCS1, ECCS0	BCH Status	00: no error was detected during the execution of PAGE_READ (13H) command. 01: errors were detected and corrected. 10: Uncorrectable errors were detected. 11: 8 bits errors were detected and corrected. Errors over 8 bits cannot be corrected. **Notes: Causes for reset:** The bit is cleared at the beginning of the PAGE_READ (13H) command. The bit indicates the loading results of Block 0 and Page 0 after powering up and reset. (The reset command (FFH) and powering up will automatically loads Block 0 and Page 0 to the cache.)

13.3 Bad Block Management

This NAND Flash device is specified to have the minimum number of valid blocks (NVB)of the total available blocks per die shown in the table below. This means the devices may have blocks that are invalid when shipped from the factory. An invalid block is one that contains at least one page that has more bad bits than can be corrected by the minimum required ECC. Additional bad blocks may develop with use. However, the total number of available blocks will not fall below NVB during the endurance life of the product.

Although NAND Flash memory devices may contain bad blocks, they can be used reliably in systems that provide bad-block management and error-correction algorithms. This ensures data integrity. Internal circuitry isolates each block from other blocks, so the presence of a bad block does not affect the operation of the rest of the NAND Flash array.

NAND Flash devices are shipped from the factory erased. The factory identifies invalid blocks before shipping by attempting to program the bad-block mark into every location in the first page of each invalid block. It may not be possible to program every location in an invalid block with the bad-block mark. However, the first spare area location in each bad block is guaranteed to contain the bad-block mark. See the following table for the bad-block mark.

System software should initially check the first spare area location for non-FFh data on the first page of each block prior to performing any program or erase operations on the NAND Flash device. A bad-block table can then be created, enabling system software to map around these areas. Factory testing is performed under worst-case conditions. Because invalid blocks may be marginal, it may not be possible to recover the bad-block marking if the block is erased. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block up to 1K program/erase cycles.

Table13-5. Bad Block Mark information

Description	**Density**	**Requirement**
Minimum number of valid blocks (NVB)	1G	1002
Total available blocks per die	1G	1024
First spare area location		Byte 1024_{th}
Bad-block mark		00h(use non FFH to check)

13.4 Internal ECC

SPI NAND FLASH provides data protection by offering internal ECC. The ECC can be enabled by setting feature bit ECC_EN. The default ECC_EN is enabled (ECC_EN = 1) after power-up and reset. Users can perform the following command sequence to enable or disable the ECC_EN.

Issue the SET FEATURES (1FH) command;

Set ECC_EN to 1 to enable ECC; set ECC_EN to 0 to disable ECC.

After the ECC is enabled and during a PROGRAM operation, the device calculate an ECC code on the 2K data in the cache and then write them into the NAND FLASH. During a READ operation, the device decodes the 2K data read out from the NAND FLASH with ECC, then write them in the cache, and show the decoding results in the ECCS1 and ECCS0. For the pages that have been erased but not programmed, the ECCS1 and ECCS0 will always be 0 during a READ operation no matter ECC_EN is 0 or 1. See Table 13-6 for more details.

Table 13-6 ECC Protection and Spare Area

Min Byte Address	Max Byte Address	ECC Protected	Area	Size	Description
000h	1FFh	Yes	Main 0	512	User data 0
200h	3FFh	Yes	Main 1	512	User data 1
400h	5FFh	Yes	Main 2	512	User data 2
600h	7FFh	Yes	Main 3	512	User data 3
800h	802h	Yes	Spare 0	3	User Meta data 0 (800H is also for Bad Block Mark)
803h	80Fh	Yes		13	ECC for Main 0 and Spare 0
810h	812h	Yes	Spare 1	3	User Meta data 1
813h	81Fh	Yes		13	ECC for Main 1 and Spare 1
820h	822h	Yes	Spare 2	3	User Meta data 2
823h	82Fh	Yes		13	ECC for Main 2 and Spare 2
830h	832h	Yes	Spare 3	3	User Meta data 3
833h	83Fh	Yes		13	ECC for Main 3 and Spare 3

Notes:
When enable ECC, the write-in data to ECC area will be ignored.

13.5 Block Protection

Table 13-7 Protection Register

Register	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Protection	A0H	BRWD	Reserved	BP2	BP1	BP0	INV	CMP	Reserved
—	—	Read & Write	—	Read & Write	Read & Write	Read & Write	Read & Write	Read & Write	Read & Write

Issue GET FEATURES (0FH) and SET FEATURES (1FH) commands to read or set the Protection Register.

SPI NAND provides write protection for all device or portion of the blocks, and all blocks are under the default write protection after power-up (BP2, BP1, BP0 = 1).

When BRWD is 1 and WP# is low, all protected bits cannot be altered by the SET FEATURES (1FH) command.

PROGRAM/ERASE command being issued to a locked block will lead to operation error (P_FAIL= 1/EFAIL= 1).

See Table 13-8 for the protected page address of the write protection bits (BP0, BP1, BP2，INV, CMP) of different capacity (take the 64-page-per-block Flash as an example).

Table 13-8 Block Lock Register Block Protect Bits(64 pages per block)

CMP	INV	BP2	BP1	BP0	Protect page Address （2048 Blocks）	Protect Rows
X	X	0	0	0	None	UNLOCK
X	X	1	1	1	00000H-1FFFFH	LOCK
0	0	0	0	1	1F800H-1FFFFH	H 1/64
0	0	0	1	0	1F000H-1FFFFH	H 1/32
0	0	0	1	1	1E000H-1FFFFH	H 1/16
0	0	1	0	0	1C000H-1FFFFH	H 1/8
0	0	1	0	1	18000H-1FFFFH	H 1/4
0	0	1	1	0	10000H-1FFFFH	H 1/2

Table 13-8 Block Lock Register Block Protect Bits(64 pages per block) (Continued)

CMP	INV	BP2	BP1	BP0	Protect page Address (2048 Blocks)	Protect Rows
0	1	0	0	1	0000H-07FFH	L 1/64
0	1	0	1	0	0000H-0FFFH	L 1/32
0	1	0	1	1	0000H-1FFFH	L 1/16
0	1	1	0	0	0000H-3FFFH	L 1/8
0	1	1	0	1	0000H-7FFFH	L 1/4
0	1	1	1	0	0000H-FFFFH	L 1/2
1	0	0	0	1	0000H-1F7FFH	L 63/64
1	0	0	1	0	0000H-1EFFFH	L 31/32
1	0	0	1	1	0000H-1DFFFH	L 15/16
1	0	1	0	0	0000H-1BFFFH	L 7/8
1	0	1	0	1	0000H-17FFFH	L 3/4
1	0	1	1	0	0000H~003FH	Block0
0	1	0	0	1	0800H-1FFFFH	H 63/64
0	1	0	1	0	1000H-1FFFFH	H 31/32
0	1	0	1	1	2000H-1FFFFH	H 15/16
0	1	1	0	0	4000H-1FFFFH	H 7/8
0	1	1	0	1	8000H-1FFFFH	H 3/4
0	1	1	1	0	0000H~003FH	Block0

13.6 Block 0 Page 0 Automatically Loads to Cache

SPI NAND will automatically load the data in Block 0 Page 0 with ECC decode during power-up process. Data can be read out of the cache by using the READ FROM CACHE (03H/0BH/3BH/6BH/BBH/EBH) command.

When the SPI NAND wake up from sleep mode it will also load the data in Block 0 Page 0 to the cache with ECC decode.

14 Power-up Sequence

At Power-up and Power-down, the device must not be selected (that is Chip Select (S) must follow the voltage applied on V_{CC}) until V_{CC} reaches the correct value:

- V_{CC}(min) at Power-up, and then for a further delay of t_{VSL}
- V_{SS} at Power-down

To avoid data corruption and inadvertent write operations during Power-up, a Power On Reset (POR) circuit is included. The logic inside the device is held reset while V_{CC} is less than the POR threshold value, V_{WI} – all operations are disabled, and the device does not respond to anyinstruction.

Moreover, the device ignores all Write Enable (WREN), Page Program, Block Erase (BE), OTP Program instructions until a time delay of t_{PUW} has elapsed after the moment that V_{CC} rises above the V_{WI} threshold. However, the correct operation of the device is not guaranteed if, by this time, V_{CC} is still below V_{CC}(min). No Write Status Register, Program or Erase instructions should be sent until the later of:

- t_{PUW} after V_{CC} passed the V_{WI} threshold
- t_{VSL} after V_{CC} passed the V_{CC}(min) level

These values are specified in Table 14-1.

If the delay, t_{VSL}, has elapsed, after V_{CC} has risen above V_{CC}(min), the device can be selected for READ instructions even if the t_{PUW} delay is not yet fully elapsed. At Power-up, the device is in the following state:

- The device is in the Standby mode (not the Deep Power-down mode).
- The Write Enable Latch (WEL) bit is reset.
- The Operation In Progress (OIP) bit is reset.

Normal precautions must be taken for supply rail decoupling, to stabilize the V_{CC} feed. Each device in a system should have the V_{CC} rail decoupled by a suitable capacitor close to the package pins. (Generally, this capacitor is of the order of 100 nF).

At Power-down, when V_{CC} drops from the operating voltage, to below the Power On Reset (POR) threshold value, V_{WI}, all operations are disabled and the device does not respond to any instruction. (The designer needs to be aware that if a Power-down occurs while a Write, Program or Erase cycle is in progress, some data corruption can result.)

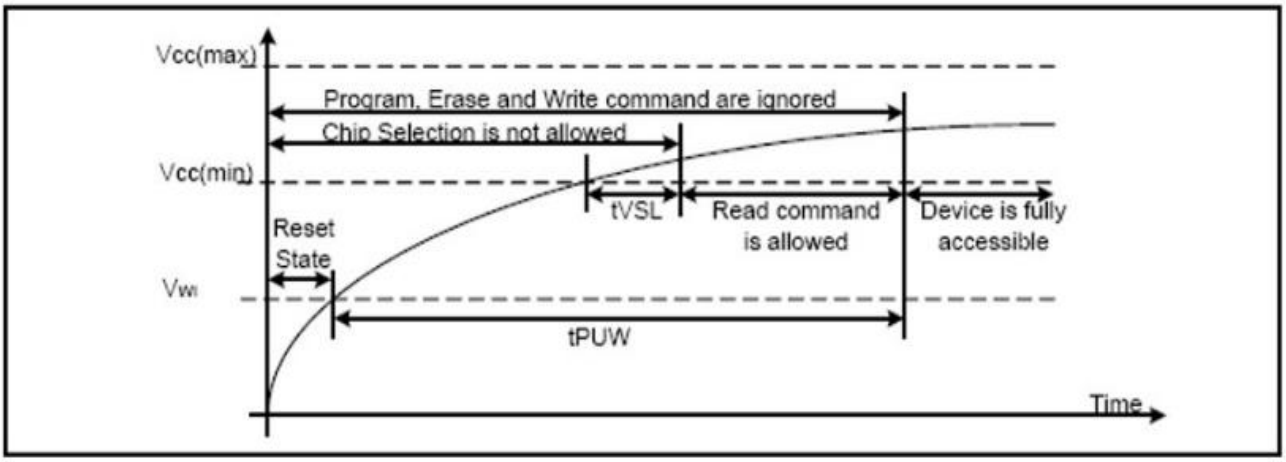


Figure 14-3 Power on Timing Sequence

Table 14-1.Power- on timing and Write Inhibit Threshold for 3.3V

Symbol	Parameter	Min.	Max.	Unit
$t_{VSL(1)}$	VCC(min) to CS# low		1	ms
$t_{PUW(1)}$	Time delay from $VCC_{(w)}$ to Write instruction		1.5	ms
$V_{W(1)}$	Write Inhibit voltage		2.9	V

Notes:

These parameters are characterized only.

15 Electrical Specifications

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to relevant quality documents.

Table 15-1 Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
T_{STG}	Storage temperature	–55	125	°C
T_{OPA}	Operation temperature (ambient)	0	70	°C
V_{CC}	Supply voltage	–0.6	4.6	V
V_{IO}	Input and output voltage (with respect to ground)	–0.6	V_{CC} + 0.4	V
V_{ESD}	Electrostatic discharge voltage (Human Body model) (1)	–2000	2000	V

Notes:

(1) JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 Ω, R2=500 Ω)

During infrequent, nonperiodic transitions and for periods less than 20ns, voltage potential between VSS and VCC may undershoot to –2.0V or overshoot to VCC_MAX + 2.0V

15.1 DC and AC Parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC Characteristic tables that follow are derived from tests performed under the Measurement Conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 15-2 Operating conditions

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply voltage		2.7	3.6	V
T_A	Ambient operating temperature	C(Commercial)	0	70	°C
		E(Extended)(1)	-30	85	°C
		I (Industrial)(1)	-40	85	°C

Notes:

(1) Please confirm with TONGYA SEMICONDUCTOR solution for the available schedule.

Table 15-3 Data retention and endurance

Parameter	Condition	Min.	Max.	Unit
Erase/Program cycles			100,000	cycles per sector
Data Retention			10	years

Table 15-4 AC measurement conditions

Symbol	Parameter	Min.	Max.	Unit
CL	Load capacitance	40(30pF/90MHz)		pF
	Input rise and fall times		5	ns
	Input pulse voltages	0.2VCC to 0.8VCC		V
	Input timing reference voltages	0.3VCC to 0.7VCC		V
	Output timing reference voltages	VCC / 2		V

Notes:

Output Hi-Z is defined as the point where data out is no longer driven.

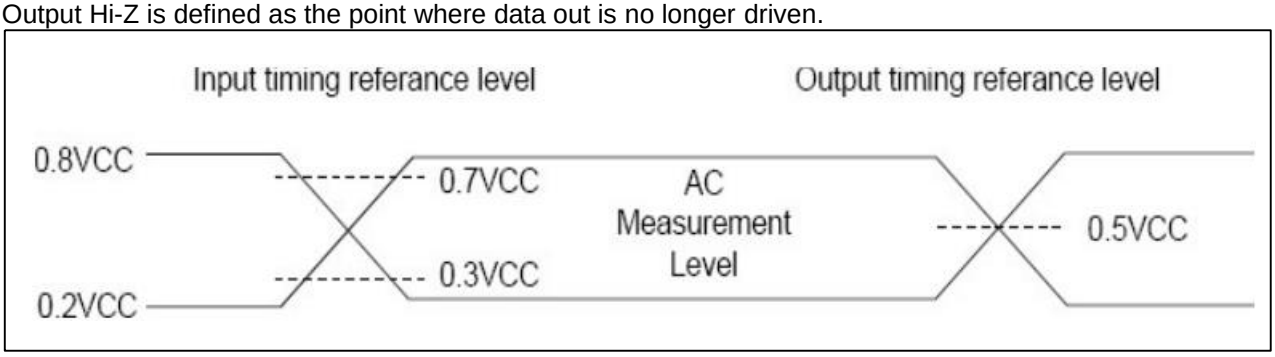


Figure 15-1. AC measurement I/O waveform

Table 15-5 Capacitance Measurement Conditions (1)

Symbol	Parameter	Min	Typ	Max	Unit	Condition
CIN	Input Capacitance			6	pF	
COUT	Output Capacitance			10	pF	
C_L	Load Capacitance			30	pF	
	Input Rise And Fall time			5	ns	
	Input Pulse Voltage	0.2*VCC		0.8*VCC	V	
	Input Timing Reference Voltage	0.3*VCC		0.7*VCC	V	
	Output Timing Reference Voltage		0.5*VCC		V	

Notes:

Sampled only, not 100% tested, at TA = 25 °C and a frequency of 20 MHz.

16 Electrical Characteristics

16.1 DC Characteristics

Table 16-1 DC characteristics

Symbol	Parameter	Test condition	Min.	Max.	Unit
ILI	Input leakage current			± 10	µA
ILO	Output leakage current			± 10	µA
ICC1	Standby current	CS# = VCC, VIN = VSS or VCC	10	100	µA
ICC3	Operating current (READ)	SCLK = 0.1VCC / 0.9.VCC	10	20	mA
ICC4	Operating current (Program)	CS# = VCC	10	20	mA
ICC5	Operating current (Block Erase)	CS# = VCC	10	20	mA
VIL	Input low voltage		-0.5	0.3xVCC	V
VIH	Input high voltage		0.7xVCC	Vcc + 0.4	V
VOL	Output low voltage	IOL = 1.6mA		0.4	V
VOH	Output high voltage	IOH = –100 µA	VCC – 0.2		V

Notes:
1. Typical values are given for TA = 25 °C.
2. These parameters are verified in device characterization and are not 100% tested.

16.2 AC Characteristics

Table 16-2 AC characteristics

Symbol	Parameter	Min	Typ	Max	Unit
F_C	Serial Clock Frequency For: all command			**90**	MHz
t_{CH}	Serial Clock High Time	5.5			ns
t_{CL}	Serial Clock Low Time	5.5			ns
t_{CLCH}	Serial Clock Rise Time(Slew Rate)	0.5			V/ns
t_{CHCL}	Serial Clock Fall Time(Slew Rate)	0.5			V/ns
t_{SLCH}	CS# Active Setup Time	5			ns
t_{CHSH}	CS# Active Hold Time	5			ns
t_{SHCH}	CS# Not Active Setup Time	5			ns
t_{CHSL}	CS# Not Active Hold Time	5			ns
t_{SHSL}/t_{CS}	CS# High Time	20			ns
t_{SHQZ}	Output Disable Time			10	ns
t_{CLQX}	Output Hold Time	1			ns
t_{DVCH}	Data in Setup Time	3			ns
t_{CHDX}	Data in Hold Time	5			ns
t_{HLCH}	Hold# Low Setup Time(relative to Clock)	5			ns
t_{HHCH}	Hold# High Setup Time(relative to Clock)	5			ns
t_{CHHL}	Hold# Low Hold Time(relative to Clock)	5.5			ns
t_{CHHH}	Hold# High Hold Time(relative to Clock)	5.5			ns
t_{HLQZ}	Hold# Low to High-Z Output			10	ns
t_{HHQX}	Hold# High to Low-Z Output			10	ns
t_{CLQV}	Clock Low to Output Valid			9	ns
t_{WHSL}	WP# Setup Time Before CS# Low	20			ns
t_{SHWL}	WP# Hold Time After CS# High	100			ns

Notes:
1 Typical values given for TA = 25°C.
2 tCH + tCL must be greater than or equal to 1/ fC
3 Value guaranteed by characterization, not 100% tested in production.

16.3 Performance Characteristics

Table 16-3 Performance characteristics

Symbol	Parameter	Typ	Max	Unit
t_{RST}	CS# High To Next Command After Reset (FFH)		500	us
t_{RD}	Read From Array(Internal ECC Disable)		25	us
	Read From Array(Internal ECC Enable)		**80**	us
t_{PROG}	Page Program Time	400	700	us
t_{BERS}	Block Erase Time	2	4	ms
tRST	After Reset, Recovery time for RD/PGM/Erase	Max 10/50/500		us
NOP	Number of partial programming operation supported	-	4	-

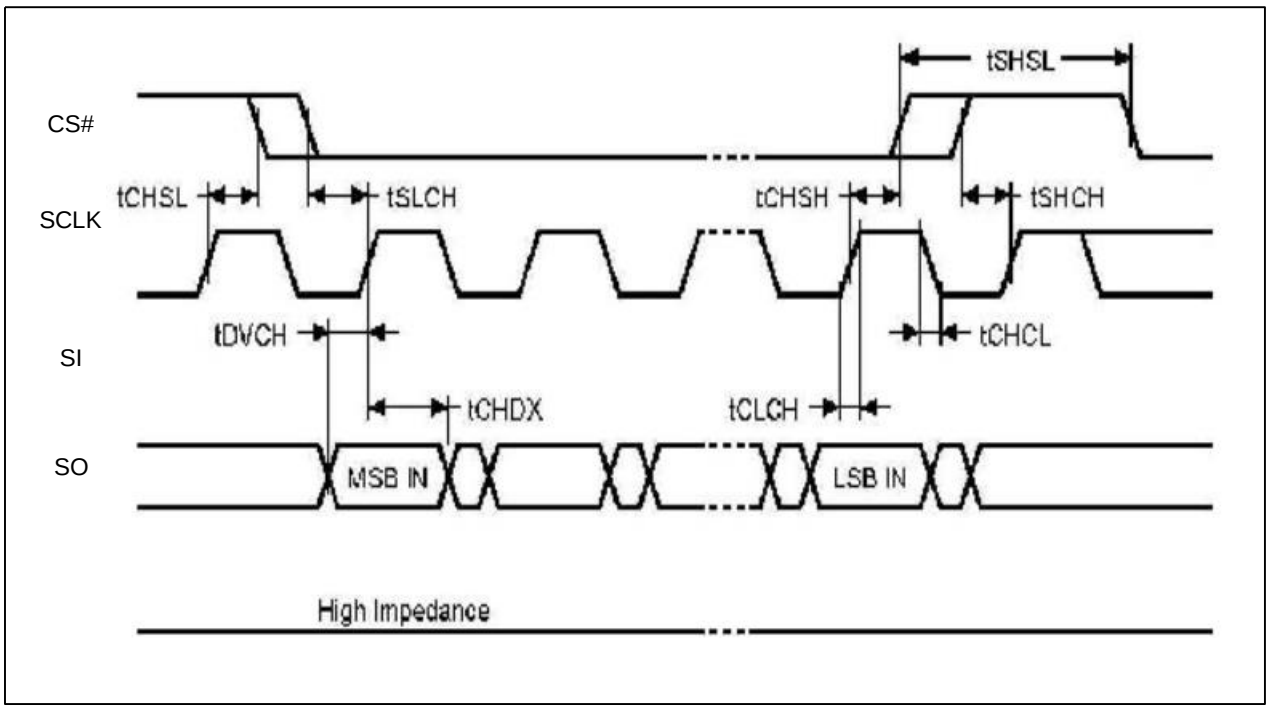


Figure 16-1 Serial input timing

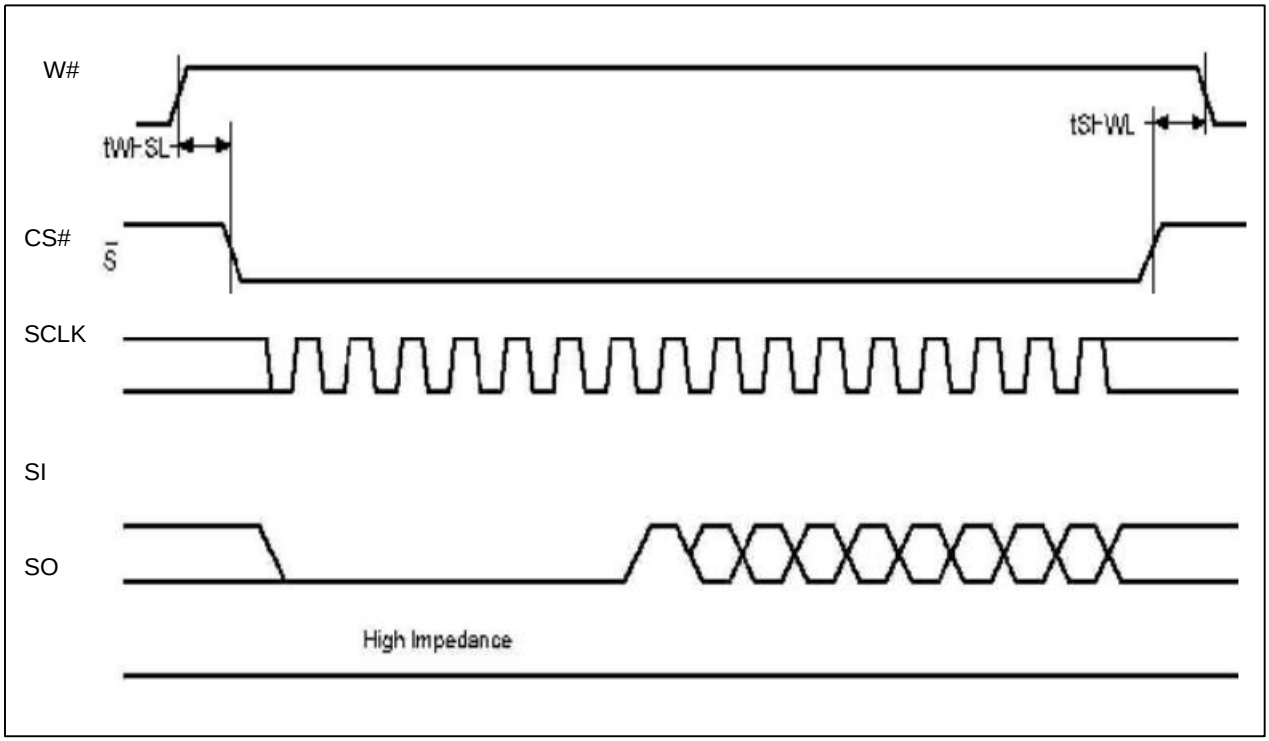


Figure 16-2 Write protect setup and hold timing

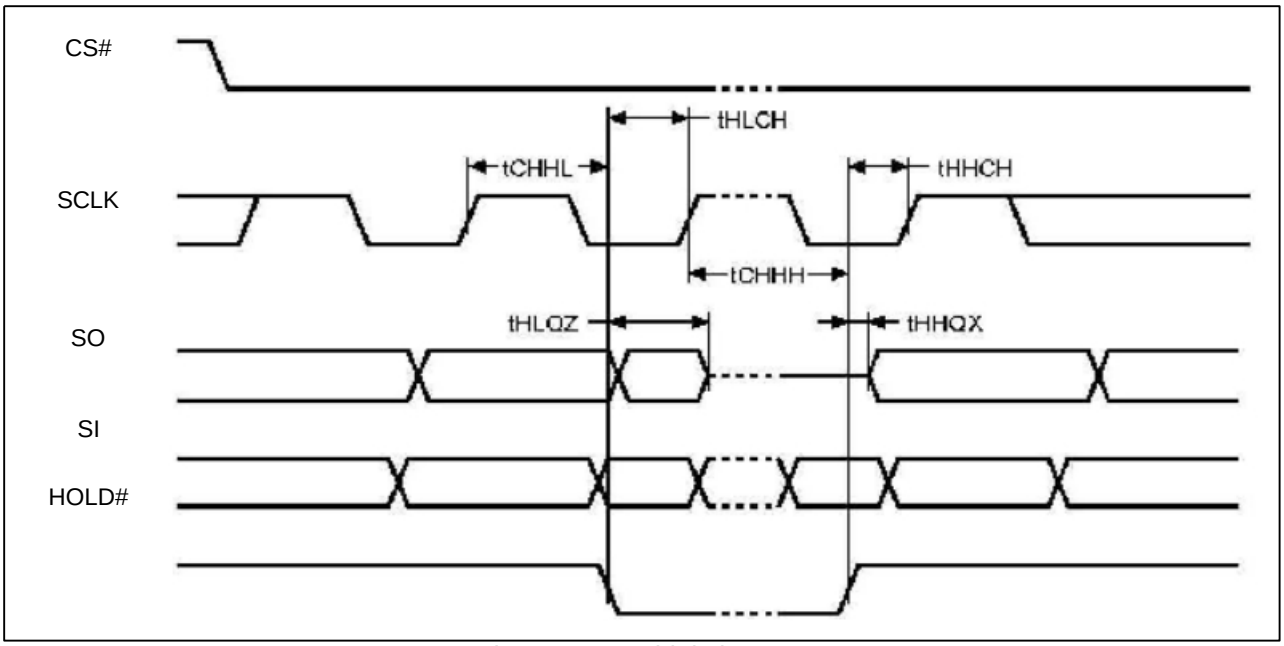


Figure 16-3 Hold timing

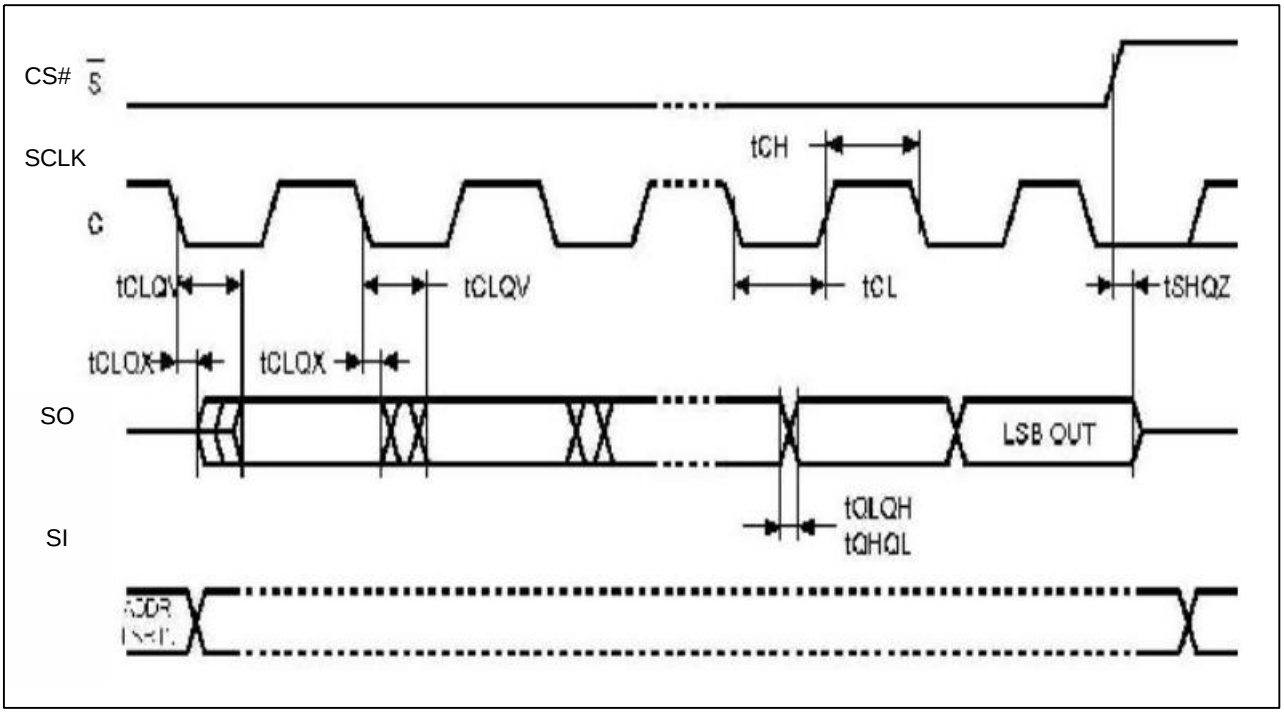


Figure 16-4 Output timing

17 Package Mechanical

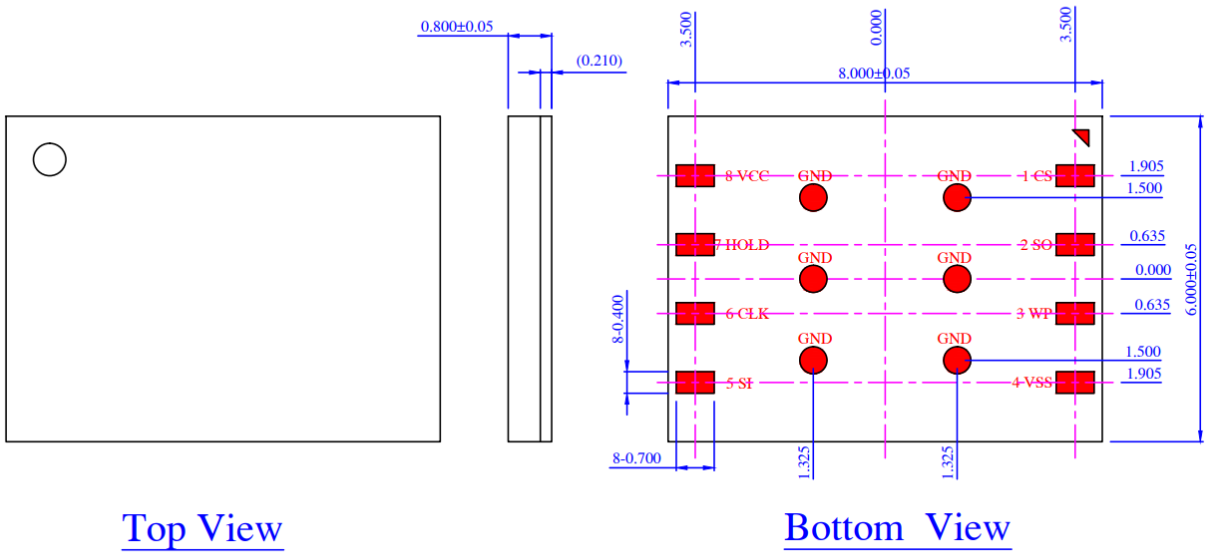


Figure 17-1 LGA 6X8mm